The Heart of ATLAS

Commissioning and Performance of the ATLAS Silicon Tracker

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EEN WETENSCHAPPELIJKE PROEVE OP HET GEBIED VAN DE
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[1] The figures in the bottom right corner of the pages represent a simulated collision event viewed along the beam-pipe. The event is one in which a microscopic-blackhole was produced and decayed immediately.

To mum and dad
In loving memory of my grandparents

"There is no success without a struggle."

Contents

Introduction

“Nothing exists except atoms and empty space; everything else is opinion.”

Democritus

The Greeks formed the basis for western thinking about our natural world up until the 17th century when chemistry came into place. Based not upon experimental reasoning, but instead, purely on philosophical grounds, they had a strong belief in a very simplistic world, in the sense that there would only be a few aspects fundamental to all matter and phenomena surrounding us. Democritus, far ahead from his time, proposed that there was one elementary particle which could not be divided into anything smaller. He named it the “atom” (derived from the Greek meaning of “indivisible.”)

However, in the 19th century, physicists soon discovered that the atom was, in fact, divisible. It was found to be composed of various subatomic particles, thanks to various experiments that had taken place. The constituents, called the electrons, protons and neutrons, were found to be able to exist independently from each other. Later, after more experimentation, new results led to the fact that the constituents of the atom could be broken down even further, to quarks.

The physics dedicated to the study of the fundamental constituents of matter and their interactions is called particle physics. The *Standard Model* of particle physics describes the interactions between elementary particles. It predicts a particle called the Higgs Boson, that provides an answer to the question:*"Where does the mass of particles originate from?"*

The advancement of particle physics today has very much to do with the new instruments and technology that have come about with time. Experience from older particle accelerators has been carried through to today’s science. The Large Hadron Collider in Geneva, Switzerland is currently the world’s largest particle collider, superseding the Tevatron in Chicago. One of the detectors located on the LHC ring is the ATLAS experiment, with the Silicon Tracker at the heart of the detector.

The semiconductor detectors in high energy physics provide precision measurement of particle tracks. When placed within a magnetic field, the particles follow a curved track allowing a highly accurate momentum measurement. Semi-conductor detectors can provide a position measurement with an accuracy of several μm, making it possible to detect secondary decay vertexes of short lived particles.

This thesis will describe all aspects of the Semi-Conductor Tracker (SCT) from prototype to macro-assembly and the commissioning period. We will begin with an introduction to the Standard Model, as well as an overview of the ATLAS detector. The remaining chapters will concentrate solely on work related to the Semi-Conductor Tracker. Chapter 3 introduces the basics of using silicon detectors to track charged particles. Using these concepts, the SCT sensors are described, stating the motives for their design. The other components which make up an SCT detector module are described.

Chapter 4 discusses the electronics used to communicate data to and from the modules. The control and monitoring software is reviewed and the steps necessary to calibrate the detector as well as to optimise the communications are discussed.

Chapter 5 aims to give an insight into each step of the assembly chain of SCT Endcap-A. It explains the entire test sequence which has resulted in a well within specification detector. Chapter 6 focuses on the performance of Endcap-A. The results include all stages of testing, both at Nikhef and at CERN.

Chapter 7 gives a detailed description of electrical noise in the modules, giving particular focus to the dependence on bias voltage. The total-strip capacitance is an important contributing factor and is discussed extensively. A noise model is introduced which describes both the front-end and sensor noise components. Using an accurate noise model, the evolution of different module parameters with the required radiation dose can be monitored. The depletion voltage is especially interesting since its rise limits the detector lifetime.

The final chapter discusses the results obtained from a global ATLAS detector cosmic run. Cosmic rays are particularly useful for commissioning purposes of each of the ATLAS sub-detectors. They provide an important method for testing the detector performance and entire readout chain. The experience gained in operating and commissioning the detector is discussed. The results of studies of the noise performance, detector response and the reconstruction software are presented.

CHAPTER 1

THEORY

"If I could remember the names of all these particles I'd be a botanist."

Enrico Fermi

Contents

1.1 The Standard Model

1.1.1 Building blocks of matter

H*adrons* can be divided into two types: integer spin *bosons* and half-integer spin *fermions*. Bosons are based on the Bose-Einstein distribution, while the fermions obey the exclusion principle, based on the Fermi-Dirac distribution. Hadrons are composed of *quarks*, which are still believed to be genuinely fundamental particles. Quarks are defined by their flavour and carry color charge, making them strongly interacting particles. Colour neutral *meson* composites are composed of quark-antiquark pairs, whilst *baryons* are made up of quark triplets. There are three generations of quarks, each with its own anti-particle, up, down, charm, strange, top, bottom:

$$\begin{pmatrix} u \\ d \end{pmatrix}, \begin{pmatrix} c \\ s \end{pmatrix}, \begin{pmatrix} t \\ b \end{pmatrix}. \tag{1.2}$$

The quarks are also electrically charged and have weak isospins and hence can also interact with other fermions both electro-magnetically and via the weak nuclear force. The lightest, most stable quark composite is the proton, consisting of two ups and one down.

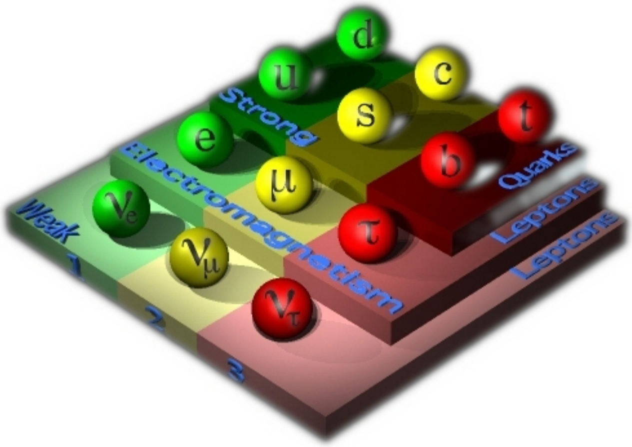


Figure 1.1: A picture of the three families of quarks and leptons and their mediating forces.

Leptons are also fermions. They too exist in isospin pairs and are grouped into three generations. The electron (e), muon (μ) and tau (τ) particles each have a distinct counterpart; a small non-zero mass, chargeless neutrino.

$$\begin{pmatrix} \nu_e \\ e \end{pmatrix}, \begin{pmatrix} \nu_\mu \\ \mu \end{pmatrix}, \begin{pmatrix} \nu_\tau \\ \tau \end{pmatrix}. \tag{1.3}$$

They are spin half fermions and interact via the weak force. All six leptons do not carry color charge. The e, μ and τ are all electrically charged and can therefore interact electromagnetically. Their associated neutrinos are charge-less and are influenced purely by the weak nuclear force. The electron is the most stable leptonic particle compared to the μ and τ which are heavier and are found in decay processes.

1.1.2 Forces

The interaction of particles is made possible by the four fundamental forces, Strong, Electromagnetic, Weak and Gravity. The exchange of an inter-mediating spin 1, gauge boson allows the transmission of forces between particles. The standard model accounts for three of the four fundamental forces present in the universe. In attributing a relative strength to the four fundamental forces, it has proved useful to quote the strength in terms of a coupling constant, α. The coupling constant for each force is a dimensionless constant.

> **Strong:** The gluons *(g)* are the mediating particles for the strongest of forces, binding together quarks. They are massless particles with a coupling constant, α_s. A nucleus is a good example of the presence of the strong force. It is responsible for holding the protons and neutrons together, forming a nucleus inside an atom. The strength of the force increases the further apart the particles are from each other. This is why one single quark has never been seen on its own, since separating them would require a vast amount of increasing energy.
>
> **Electro-magnetic:** The photon, (γ) is the force carrier for electro-magnetic forces. It is a massless particle with a coupling constant, $\alpha = \frac{1}{137}$. An example would be electrons orbiting an atom. Unlike the strong force, it acts over a long range.

> **Weak**: Its mediating particles are the $W^{\pm}$ and Z^0 which act over a very small range. The weak charged bosons have a mass of ≈80 GeV and the neutral Z boson, a mass of ≈91 GeV. An example of the weak force is radioactive decay.
>
> **Gravity:** This is the force most apparent in everyday life. It is however, so small in comparison to the other forces, that it is neglected. The gravitational coupling constant, $\alpha_g = 10^{-39}$. It is not included in the standard model.

The Standard Model theory suggests that at very high temperatures where particle energies are in excess of 100 GeV, the weak and electromagnetic interactions are manifestations of a single force. The electro-magnetic mediator, the photon, is massless, and the weak force mediators $W^{\pm}, Z^0$ bosons are more than 80 times that of a proton. The difference in masses is attributed to spontaneous symmetry breaking. A symmetry-breaking mechanism was introduced called the Higgs field, requiring a new boson, the Higgs, to mediate it [51, 52].

1.1.3 Higgs Boson

The Higgs mechanism was proposed in 1964 by Peter Higgs, Francois Englert and Robert Brout. The theory suggested that all particles have zero mass moments after the creation of the universe. As the universe cooled and the temperature falls below a critical temperature, an invisible field permeating space appears, known as the "Higgs field", and with it an unstable massive particle called the "Higgs boson". When a particle interacts with this field, it acquires a certain amount of mass. The longer a particle interacts with this field, the heavier it becomes. Those particles that do not interact, simply remain massless.

The Standard Model allows a prediction of production cross sections and branching ratios, assuming the particle exists with a certain mass. The value of this mass is unknown, however using experimental data based on previous and current particle experiments, constraints have been determined for the Higgs mass. The Large Electron Positron collider (LEP) [59] established a lower limit of $M_H > 114$ GeV at a 95% confidence level [54]. More recently, combining data from both CDF [19] and DØ [27] experiments at the Tevatron in Fermilab, have excluded a Higgs mass of 170 GeV at 95% confidence level [48] (see section 1.2.1 for details).

1.2 Circular Colliders

In order to investigate nature at its smallest scales, the use of a particle accelerator is essential. Present day accelerators can provide controlled beams with high precision, and most importantly, with high energies. The “de Broglie wavelength” of a moving particle can be related to its momentum. The more energy (momentum) at particle has, the greater the exploration of nature at small scales.

There are a number of important factors to consider which will influence new discovery potential. Here only a few will be mentioned briefly. For a good overview of accelerator performance challenges see references [77, 63, 16]. There are the design limits of the detector itself, the design limitations due to the beam physics and lastly, the design limits due to the collider technology. The beam energy and luminosity are two key parameters in defining the performance of a collider.

Beam Energy

When two beams collide head on, the collision energy of the beams is important. It is referred to as the centre of mass energy. The invariant mass M is a mathematical combination of a particle's energy E and its momentum p. It is equal to the particle mass in the rest frame. As an example, consider a two-beam head-on particle collision. The invariant mass of the system is defined as;

$$M^2 = (E_1 + E_2)^2 - \|\mathbf{p}_1 + \mathbf{p}_2\|^2 = (E_1 + E_2)^2 \tag{1.4}$$

Higher energy beams also require greater magnetic fields and beam radius governed by Lorentz's law:

$$p = eBR \tag{1.5}$$

where p is the beam momentum, e is the electric charge, B is the magnetic field and R is the radius of the collider ring. The technological limits of the magnets imposes a limit on the ability to bend a collision beam at a certain radius. Larger radii colliders prove too costly.

Luminosity

The second key factor is the luminosity. It is a measure of the number of particles colliding per second per effective unit area of the overlapping beams. If two beams containing k bunches and n_1 and n_2 particles collide with a revolutionary frequency f, then the luminosity is defined as:

$$\mathfrak{L} = \frac{n_1 \cdot n_2 \cdot k \cdot f \cdot}{4\pi\sigma} \tag{1.6}$$

where σ is the beam cross-sectional area. The event rate is measured by the colliders luminosity and is proportional to the interaction cross section. It expresses the number of particle collisions that take place every second. By increasing the number of particles in each bunch, the beam size and the number of bunches, the luminosity can be increased. There are, however, limitations on each of these. Several factors contribute to the degradation of the beam luminosity. In the next section a few of the main problems are discussed [35].

At each experiment location, in the centre of the detector, the opposing proton bunches cross in order to establish proton proton collisions. However, in practice, only a small fraction of particles do collide and lead on to give an event. The rest are all deflected by the electromagnetic field coming from the opposing bunch. On each revolution of the tunnel these deflections accumulate increasing the risk of particle loss. This is known as the "beam-beam" effect. If too many particles are crammed into a single bunch, the stability of the particles within the beam becomes extremely difficult. This therefore imposes a limit on the number of particles within each bunch. By increasing the number of bunches within a beam cycle, this imposes requirements on the resolution of the electronic technology reading out each event. The technology drives the limit for the speed to which the correct event can be read out.

Another problem that occurs during beam acceleration is that each of the 2835 proton bunches leaves behind an electromagnetic wake field which leads to interference in each successive bunch. These collective instabilities lead, in turn, to beam loss. In addition the guiding and focusing magnetic fields of the accelerator cause a de-stabilising effect on the motion of the particles, making their trajectories more chaotic. Therefore after a large number of revolutions, this effect accumulates causing particles to be lost.

The emittance of the beam is a measure of the area occupied by a beam in phase space. Keeping the emittance small means that the likelihood of particle interactions will be greater resulting in higher luminosity. A low emittance particle beam is a beam where the particles are confined to a small distance and have nearly the same momentum. The last limiting parameter of the collider performance to be discussed is the duty cycle of the beam. It is an important factor since it defines the lifetime that the colliding beam is on for, and therefore controls the number of particle interactions in one beam cycle. Power consumption would be too high for a beam to be on continuously.

The Large Hadron Collider

Situated between the Jura mountains in France and Lake Geneva in Switzerland, lies a tunnel 27 km in circumference, 50-125 m underground and sloping at 1.4% gradient towards Lake Geneva. Built previously in the 1980's for the Large Electron-Positron collider, the tunnel now serves a new purpose, housing what is known as the Large Hadron Collider (LHC). It is designed to produce head on collisions between two proton beams with a centre of mass energy of 14 TeV, with an exceptional luminosity of 10^{34} cm^{-2} s^{-1}. This will make the LHC the world's highest energy particle accelerator.

There are four main experiments situated around the ring at different stations: ALICE, ATLAS, CMS and LHCb (see Figure 1.2). The beams are prepared in CERN's existing accelerator complex, the Proton Synchrotron and Super Proton Synchrotron, accelerating protons up to 450 GeV. Afterwards they are injected into the LHC ring to obtain their maximum energy of 7 TeV each. To bend such sized beams, the LHC dipoles have to be able to produce magnetic fields of 8.36 T given the constraints on the circumference of the tunnel and collision energy. This is made possible with the use of superconductivity. The ability of certain superconducting materials, usually at low temperatures, allows an electric current to conduct without resistance and power losses, producing a high magnetic field. At such high energies, some 8000 superconducting magnets are used to guide and collide the beams through the vacuum chamber. The magnets must be operated in super-fluid helium at 1.9 K. Several technological challenges were met during the LHC design, one of them being the 1232 superconducting dipoles required to achieve a dipole field of 8.36 T. The design consists of two superconducting magnetic channels housed in the same yoke and cryostat.

In order to obtain such high luminosities, each proton ring is filled with 2835 bunches (groups of protons) of 1.1×10^{11} particles each. Once the maximum beam energy of 7 TeV has been reached the beams counter rotate for several hours. On each revolution, the beams are forced to collide at the experiment locations. After approximately 10 hours, the beams have degraded and the machine is emptied and refilled.

Despite certain preventative measures, a small fraction of the particles in the beam migrate towards the beam pipe walls. The energy of the particles is then converted into heat which can lead to "quenching" the magnets from their superconducting state. Should this occur to any one of the super-conducting magnets, several hours can be lost to rectify the disruption to the accelerator operation. To prevent such events from occurring a collimation system has been implemented to identify and catch any unstable particles well within a safe distance from any super-conducting components.

1.2.1 From Tevatron to the LHC

The Tevatron [75],[69] was the first super-conducting magnet, circular proton collider in the world. Up until the LHC era, it was also the highest energy proton accelerator. Located at Fermilab, Chicago, it was first commissioned in 1983. It has a 6.3 km ring, with beams circulating protons in one direction and anti-protons in the other. Collisions of are formed at the two detectors located on the ring: CDF, DØ. Each revolution of the beam consists

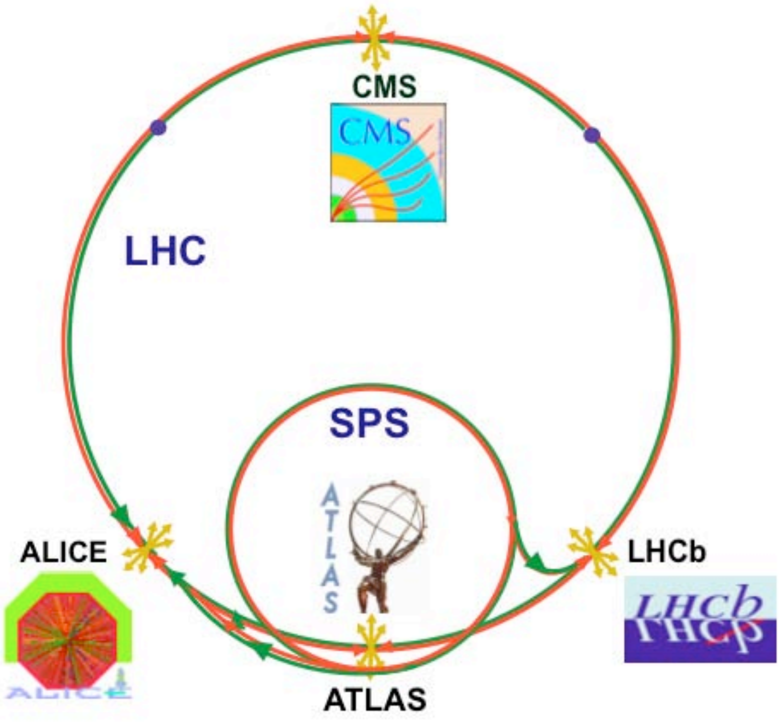


Figure 1.2: LHC and its four main experiments.

Parameter	Value
Circumference	27 km
Proton energy	7 TeV
Injection energy	0.45 TeV
Number of bunches	2835
bunch separation	25 ns
Number of protons per bunch	$1.1\times^{11}$
beam current	0.54 A
beam lifetime	10 hr
dipole field	8.36 T

Table 1.1: A summary of the main LHC parameters.

of 3 trains of 12 bunches, with a 396 ns separation. In 2002 its collision energy was at its maximum of 1.96 TeV. In general, the process of creating the $\overline{\mathrm{p}}$ is much more time consuming, taking 100,000 protons to create just one or two anti-protons. It is this $\overline{\mathrm{p}}$ creation process that is the limiting factor for the luminosity. Nevertheless, since the beginning of RunII in 2001 over 4.2 fb^{-1} were delivered.

In 1995, the collaborations announced the discovery of the top quark, and by 2007 they measured its mass to a precision of nearly 1%. In 2006, they also made the first measurement and observation of B_s oscillations. The experiences of Tevatron will be most valuable at the LHC with regards to backgrounds of Higgs searches as well as experimental techniques. Whilst the Higgs boson is yet to be found, the recent results from Tevatron exclude a mass for the Higgs of 170 GeV with 95% confidence level (see Figure1.3). This is the first time that the Tevatron experiments directly restricted the Higgs mass. These results show that CDF and DØ are both sensitive to potential Higgs signals. The Tevatron experiments will continue to collect data until year 2009, whilst the LHC experiments ATLAS and CMS at CERN are expected to record the first events in 2009, starting with a higher sensitivity due to the 14 TeV collision energy. The next years will indeed be exciting times ahead for the search of the Higgs boson.

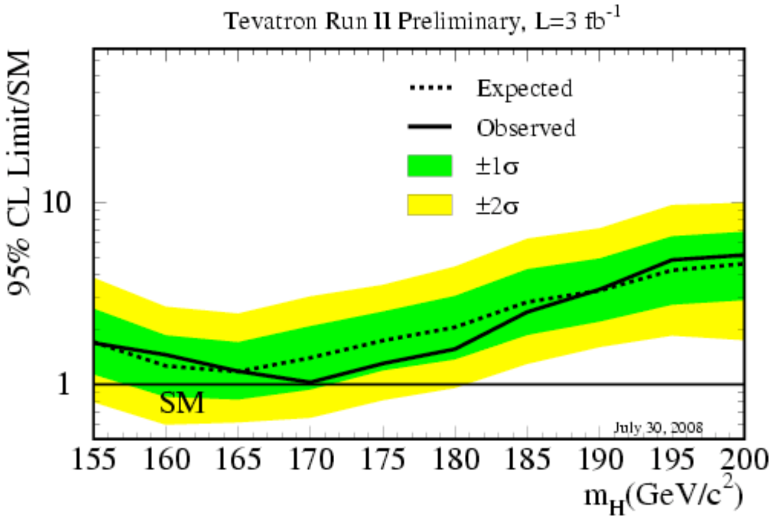


Figure 1.3: Combined data from Tevatron's CDF and DØ experiments have excluded the mass of a 170 GeV Higgs boson with a 95% confidence level [48].

1.2.2 Higgs searches at LHC

The most dominating production cross sections of a Standard Model Higgs is by gluon-gluon fusion with weak-boson fusion following second. Figure 1.4 shows the Higgs production mechanisms at the LHC in the intermediate mass range.

A **light Higgs** boson with a mass <120 GeV, can be discovered using the following

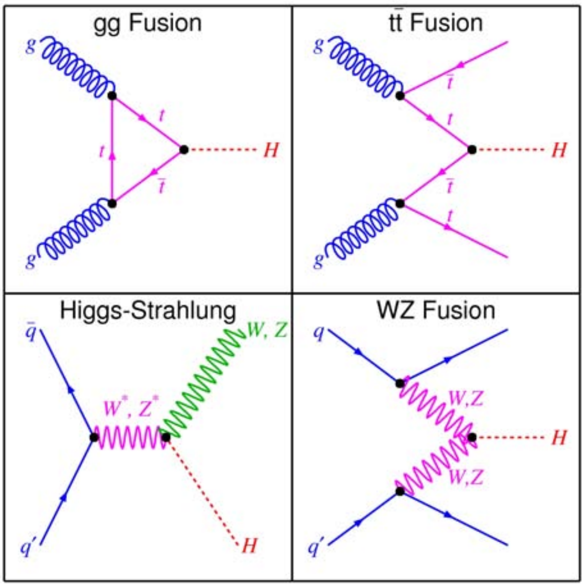


Figure 1.4: Higgs production channels.

signals:

$$H \rightarrow \gamma\gamma$$
$$\mathrm{t\bar{t}H, with\ \ H \rightarrow b\bar{b}}$$

The $\mathrm{b\bar{b}}$ decay channel gives a high branching ratio, but proves challenging due to the large backgrounds. The $\gamma\gamma$ channel has a lower branching ratio, but the background is more controlled, giving good prospects for a detectable signal. It requires an excellent performance of the EM calorimeter, since the mass resolution has to be of O(1%), if the signal is to be observed above the irreducible $\gamma\gamma$ continuum.

For the **intermediate Higgs** within the mass range 120 GeV to $2\mathrm{M_z}$ the following decays channels are important:

$$H \rightarrow ZZ^* \rightarrow l^+l^-l^+l^-$$
$$H \rightarrow \mathrm{WW}^* \rightarrow \mathrm{l}\nu\mathrm{l}\nu$$

Figure 1.5 shows the Higgs production cross sections in the 0-200 GeV mass range and Figure 1.6 gives the corresponding branching ratios for these processes. The decay process with ZZ^* is only valid up until 160 GeV, when the decay channel branching ratio reduces significantly. The background reduction is more difficult with one of the Z's being off-shell. However, in the heavier mass region (150 GeV $< \mathrm{m_H} <$ 180 GeV) the process described by WW^* becomes more dominant. The escaping neutrinos can make the precision of the mass peak measurement more difficult.

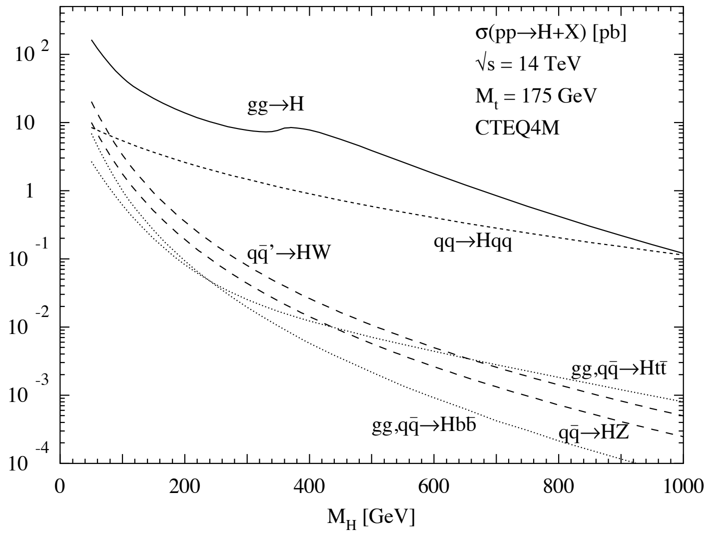


Figure 1.5: Higgs production cross-sections for the entire LHC mass range.

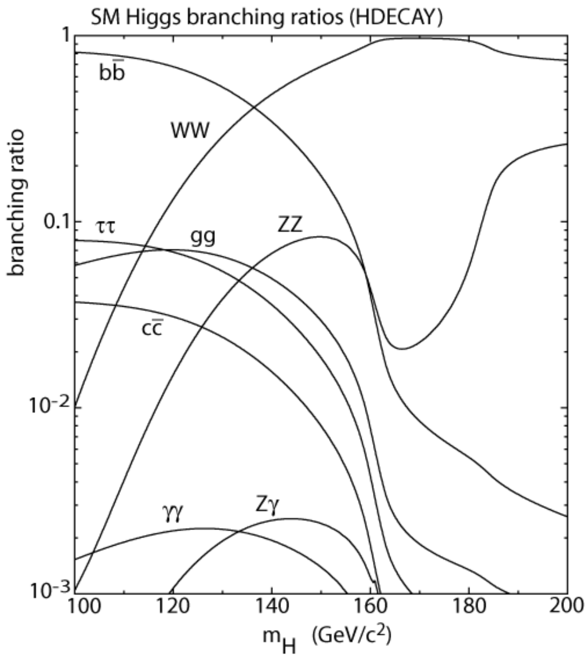


Figure 1.6: Branching ratios for Standard Model Higgs decay channels in the intermediate mass range.

Heavy Higgs decay signals can also be investigated and are sensitive over a wide mass range. For the case where $2\mathrm{m}_Z < \mathrm{m}_H < 700$ GeV, the following process is useful.

$$H \rightarrow ZZ \rightarrow l^+l^-l^+l^-$$

This is known as the "*golden channel*" since it provides a clean signature with four leptons and has a low background.

For the case of a **very heavy Higgs** in the mass range (700 GeV < m_H < 1000 GeV), there are two additional decay processes:

$$H \rightarrow ZZ \rightarrow l^+l^-\nu\overline{\nu}$$
$$H \rightarrow WW \rightarrow l\nu\mathrm{jetjet}$$

The ZZ process involves a significant portion of the missing energy due to the neutrinos. Which means that the signal will be detectable as a peak in the missing energy spectrum. The second heavy Higgs process involving WW will provide a higher branching ratio.

During the first three years, the LHC will run at an integrated luminosity of 100 fb^{-1} At such a luminosity a Standard Model Higgs discovery is possible over the full mass range up to 1 TeV. One of the experiments capable of discovering the Higgs Boson, is the ATLAS experiment. It has been designed to exploit the full range of the Higgs mass, capable of measuring it with a significance better than 5σ.

CHAPTER 2

THE ATLAS EXPERIMENT

"A life-giving factor lies at the centre of the whole machinery and design of the world."

John Wheeler

Contents

One of the largest particle detectors of our time is the ATLAS[1] detector. Designed to observe proton-proton collisions at 14 TeV, this unprecedented energy opens up a new range of experiments, probing nature at a scale of 10^{-18} m. The ATLAS collaboration consists of more than 1800 participants from over 150 institutes worldwide. The ATLAS experiment is a general purpose detector, aimed at observing new physics processes. The following criteria of the detector were given in the ATLAS Technical Proposal(1999) [11]:

- Excellent electromagnetic calorimetry for $e^{\pm}$ and γ identification and measurements, complemented by full-coverage hadronic calorimetry for accurate jet and missing energy measurements

- High precision muon momentum measurements, with the capability to guarantee accurate measurements at the highest luminosity using the external muon spectrometer alone;

---

[1] ATLAS is an acronym for A Toroidal Lhc ApparatuS.

- Efficient tracking at high luminosity for high momentum leptons, electron and photon identification, τ-lepton and heavy flavour identification, and full event reconstruction capability at lower luminosity;
- Large acceptance in η with almost full ϕ coverage everywhere;
- Triggering and measurements of particles at low momentum thresholds, providing high efficiencies for most physics processes of interest at the LHC.

The ATLAS experiment makes full use of the physics potential available within the TeV energy range provided by the LHC. At high luminosities, the physics performance of the detector with respect to the Higgs, extra dimensions and strong symmetry breaking are all very promising [76][61].

2.1 Detector overview

Standing at an enormous size – 45 m in length, 25 m high and wide and with a mass of 7000 tonnes – the ATLAS experiment is almost equivalent to the size of a five storey building, making it the largest collider experiment ever built. It is a detector at interaction point 1 on the LHC ring. The cavern, known as UX-15, is home to the detector and there are two smaller caverns on either side of the LHC ring (US-15 and USA-15) which are used for services, cooling and data acquisition. The detector layout consists of 3 major components: *Inner Detector*, *Calorimeter* and the *Muon Spectrometer*. The Inner Detector (ID) is embedded in a solenoidal magnet which generates a field of 2 Tesla. The powerful magnetic

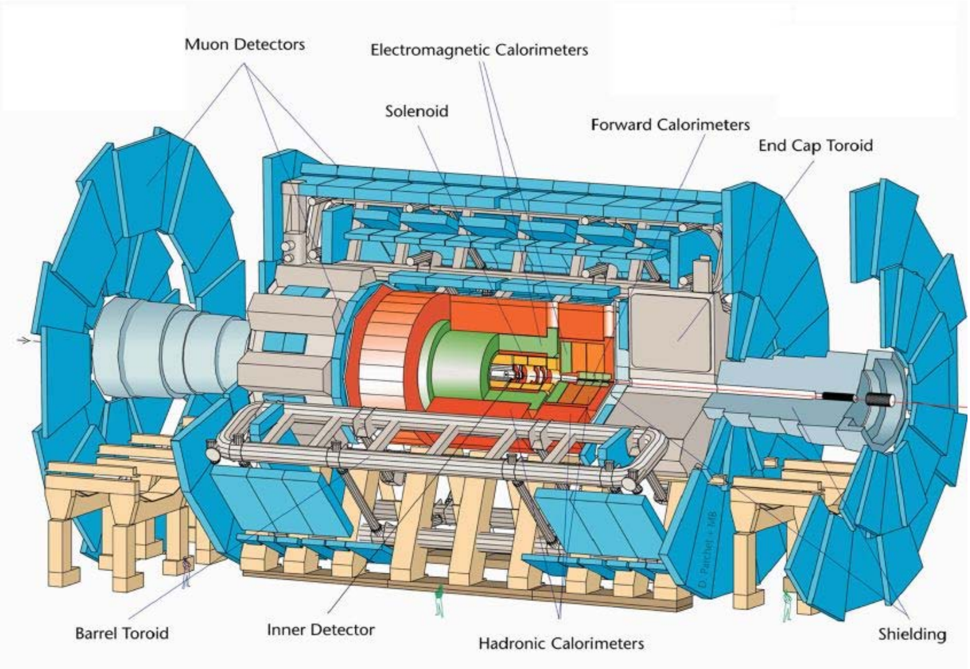


Figure 2.1: The ATLAS Detector.

field deflects the particles and the curvature of their tracks reveals the momentum and electric charge of each particle. The inner part of the tracking, which consists of high resolution silicon pixel and strip detectors, allows for momentum and vertex measurements, whilst the outer part of the ID, which consists of straw-like tracking detectors, contributes to electron identification using transition radiation as well as providing momentum measurements.

Surrounding the ID, "sampling" calorimeters measure the energies of most of the charged and neutral particles resulting from the interaction point. Liquid Argon (LAr) electromagnetic (EM) technology is used giving excellent coverage and performance over the pseudo rapidity range $\eta < 4.9$. The EM calorimeter measures the energy deposits of the e and γ's produced in the collision. This is achieved by combining closely packed absorber layers of lead with LAr as the sampling material between the plates. The thin layers of LAr "sample" the particle shower by measuring the ionisation losses of the charged particles in the shower. The careful design of the dense, absorbing plates allows a uniform response in all directions using an "accordion" like geometry.

A Hadronic Calorimeter absorbs most particles which are not stopped by the EM calorimeter. In the barrel part, scintillating plastic tiles emit light whenever a charged particle passes through the medium. Optical fibres carry the light pulses to the photo-multiplier tubes placed behind the calorimeters and convert the pulse to an electronic signal. The scintillators are interspersed by tiles of steel absorber. In the forward and endcap regions, energy measurements are taken using copper and tungsten absorbers with liquid argon technology. This is as a result of the radiation levels being so high due to the close proximity of these regions to the proton beams.

Lastly, the muon spectrometer contributes greatly to the overall size of the ATLAS Detector; the third layer of muon chambers lies approximately 23 m along the beam pipe direction from the interaction point. Muons are the only charged particles that pass through the calorimeters. The large system of superconducting magnet coils causes the trajectories of the particles to bend. The extent of the bending allows measurements of their momenta and electric charges.

2.2 Data Acquisition and Trigger

During the design luminosity run of 10^{34} cm^{-2} s^{-1}, at the start of a spill, on average 23 proton-proton collisions will occur in every bunch-bunch crossing. In order to reduce the amount of data registered, a highly efficient trigger system is needed to select only the most important events from the background. The ATLAS detector has of the order of 10^8 channels and they require an extremely complex trigger capable of identifying new, rare physics processes. With a nominal bunch crossing rate of 40 MHz, the ATLAS trigger [34] will reduce the event rate to approximately 100 Hz, writing each event to mass storage. Figure 2.2 shows the three level trigger:

1. **The Level 1 trigger**

   This receives signals from the calorimeter and muon detectors of ATLAS, reducing the event rate by a factor of 500 to 75 kHz within 2.5 μs;

2. **The Level 2 trigger**

   Unlike the first level, this level trigger is a software based selection process using algorithms. Regions of Interest (ROIs) are recognised and passed on to the level 2 trigger, allowing it to access the data from each sub-detector involved in the event. This reduces the event rate further to approximately 1 kHz;

3. **The Event Filter** Similarly using software based algorithms, the event filter waits until the entire event information has been formed before applying any cuts. In just a few seconds a thorough event selection and classification will be constructed, giving an event rate of around 100 kHz.

The level 1 trigger is a highly complex hardware system built from a calorimeter trigger, a muon trigger and a central trigger processor (CTP). The main requirement of the calorimeter trigger is to search for particular physics signatures such as high transverse energy electron, photon and tau particles, hadrons or jets. Each signature is compared to a given set of transverse energy thresholds and the multiplicity of signatures that pass the requirements is counted. There are 7200 analogue input signals from a designated trigger tower to the calorimeter trigger. The trigger tower is responsible for collating information from all the ATLAS calorimeters and has an average granularity of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$.

For every event selected, the calorimeter trigger determines the total and missing transverse energy and the results are compared to eight different thresholds for missing E_T and four for total E_T. Next, the position, type, and threshold statistics for every selected candidate are sent to the ROI for storing. These events are then selected to proceed to the high level trigger (HLT) for the next step of the selection.

Similarly the muon trigger gathers the information for the muon chambers and determines the multiplicity count for events passing through six different thresholds. Like the calorimeters, the multiplicities are given to the CTP and the regions of interest are sent to the HLT for further analysis. The main task of the CTP is to gather all the information from the calorimeters and muon triggers in order to determine the level 1 event decisions before sending the information to the HLT stating which signatures have been identified.

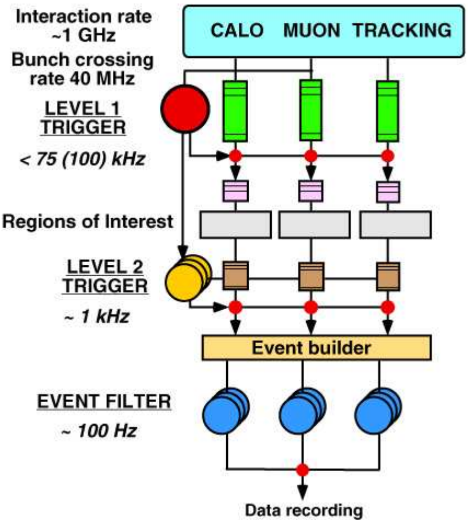


Figure 2.2: A schematic view of ATLAS trigger system.

The HLT [42] consists of the level 2 trigger and the event filter. The regions of interest identified by the level 1 are passed to the level 2 unit for validation using a step by step procedure performed using the HLT steering package. This allows for an efficient event selection process since the HLT can reject an event at any stage during the validation procedure. As a result of the regions of interest, only a small percentage of the full event data is needed for the event reconstruction in level 2. The steering is implemented using so called "trigger menus" to identify physics signatures known as trigger elements. For example, isolated particles: $e^{\pm}$ with $P_T > 25$ GeV, γ's with $P_T > 20$ GeV or pairs of isolated particles with slightly lower P_T. These trigger elements are refined by the HLT selection and at the end of the process only one output will remain, representing the hypothesis of the expected reconstruction result.

Once the entire event has been fully built it is passed on to the Event Filter Linux PC Farm. Here off-line selection algorithms have access to the complete event data, including up to date calibration and alignment software.

2.3 Muon Spectrometer

The muon spectrometer, located at the outer most layers of the ATLAS detector, has the largest detector volume. Its design allows it be an independent muon trigger as well as having the capability to reconstruct high quality, stand-alone muons. Four different chamber technologies are used, all arranged in such a way that particles produced at the interaction point will pass through three cylindrical layers (called “stations”). The layout is based upon the use of large superconducting air-core toroid magnets for the deflection of muon tracks, combined with the use of separate trigger and high precision tracking chambers. Each toroid consists of eight superconducting coils.

The spectrometer is divided into one barrel region and a transition and endcap region. Chambers are positioned cylindrically in three separate layers around the beam axis, to measure tracks. Similarly the transition and end-cap regions are arranged vertically in four layers. The barrel layers lie at radii of ~ 5, 7.5, and 10 m from the beam axis covering an $\eta \leq 1$. The end-cap chambers lie at 7.4, 10.8, 14 and 21.5 m from the interaction point covering $1 < \eta < 2.7$.

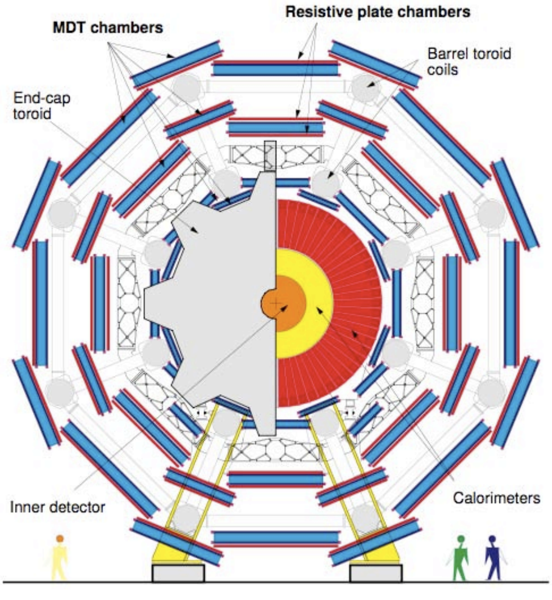


Figure 2.3: Two-dimensional view of muon spectrometer.

Monitored Drift Tubes (MDTs) and Cathode Strip Chambers (CSCs) provide a precision measurement of muon trajectories in the barrel and endcap regions. The MDTs provide co-ordinates over most of the η range, however the CSCs in the inner region $2 < \eta < 2.7$ of the first endcap wheel, provide higher granularity and are better equipped to cope with background conditions. The trigger system is provided by the other two detector technologies: Resistive Plate Chamber (RPCs) in the barrel and Thin Gap Chambers (TGCs) in the end-cap regions. Table 2.1 gives an overview of each of the four types of chambers used, as well as giving an indication of the scale of each detector type.

The MDTs consist of an aluminium tube, 30 mm in diameter, 400 μm wall thickness and a 50 μm diameter central tungsten wire. The single hit resolution is 80 μm. The

Table 2.1: Muon Chamber Overview

		Chamber resolution			Number of	
Type	Function	z/R	ϕ	time	chambers	channels
MDT	tracking	35 μm (z)	–	–	1088(1150)	339 k(354 k)
CSC	tracking	40 μm (R)	5 mrad	7 ns	32	30.7 k
RPC	trigger	10 mm (z)	10 mrad	1.5 ns	544(606)	359 k(373 k)
TGC	trigger	2-6 mm (R)	3-7 mrad	4 ns	3588	318 k

detection is based on a gas mixture of Ar/CO_2 (93%/7%), pressurised at 3 bar. The drift tubes are arranged in multilayers (3 or more single layers each) with each tube readout at one end.

A CSC is essentially a multi-wire proportional chamber, where the precision co-ordinate is determined by measuring the charge induced on the cathode as a result of the avalanche formed on the anode wire. The CSCs provide good time resolution, small e drift times (less than 30 ns), good track resolution and low neutron sensitivity.

The RPCs are much simpler to make due to the fact that there are no wires required. They are constructed from two parallel resistive Bakelite plates separated by insulating spacers, creating a narrow 2 mm gas gap. A uniform electric field of 4.5 kV/mm is used to multiply the primary ionisations. Metal strips, coupled to both sides of the detector read the signals. The readout strips are optimised for good transmission properties allowing the preservation of excellent intrinsic time resolution of $\approx$ 1.5 ns.

The TGCs are very similar in design to the CSCs but with the anode wire pitch larger than the cathode-anode distance. The chambers are operated using a highly flammable gas mixture (55% CO_2 and 45% n-pentane) requiring safe handling precautions. The gas gap has a length of 2.8 mm and an expected operating high voltage of 2.9 $\pm$ 0.1 kV. These criteria give a short drift time and good time resolution .

2.4 Calorimeters

Three types of calorimeters exist in the ATLAS experiment; Electromagnetic Calorimeter (EM), Hadronic Calorimeter and the Forward Calorimeter. The next sections will discuss these briefly.

Electromagnetic calorimetry

The EM calorimeter consists of a barrel sector and two endcaps. It uses LAr technology as the sampling material between the lead absorber plates and accordion like kapton electrodes, providing a uniform response in all directions. The barrel is split into two equal parts with a small separation of 6 mm at $z = 0$. Similarly, each endcap consists of two individual sections: an outer wheel covering $1.375 < \eta < 2.5$ and an inner wheel for $2.5 < \eta < 3.2$. In the barrel, the LAr gap is 2.1 mm however, the endcap design is somewhat more detailed due to the accordion folds increasing with the endcap radius. This, in turn, causes the LAr gaps to increase with radius. In the barrel, the total thickness of the EM calorimeter is greater than 22 radiation lengths (X_o) and greater than 24 X_o in the endcaps. Surrounding the inner detector cavity, is a barrel cryostat containing the barrel EM calorimeter. Similarly, there are two endcap cryostats housing the endcap EM, hadronic and forward calorimeters.

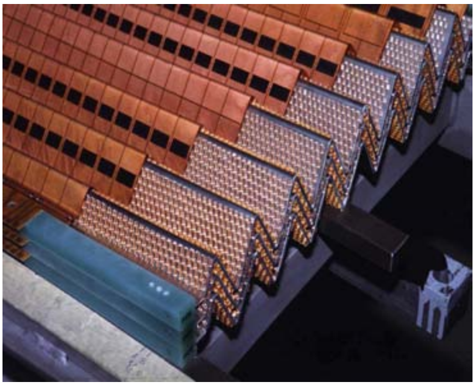


Figure 2.4: EM Calorimeter.

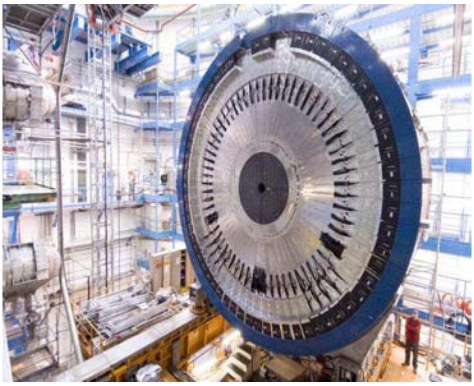


Figure 2.5: Tile Calorimeter.

In the precision physics region ($\eta < 2.5$), the EM calorimeter is split into three longitudinal sections: a strip section, a middle section and the back section. The strip sector acts as a "preshower" detector, improving particle identification as well as giving an accurate position measurement in η. To account for any electrons or photons lost in the calorimeter, there is a pre-sampler. This uses a layer of LAr in both the barrel and endcap regions. In the overlap areas between the barrel and the endcaps, scintillator tiles are added to aid the pre-sampler in the regions $1.0 < \eta < 1.6$.

Hadronic Calorimeters

To cover the wide range of $\eta < 4.9$ two different techniques are used: Tile Calorimeter and the LAr Calorimeter. The total thickness of the hadronic calorimeter is equivalent to 11 interaction lengths at $\eta = 0$, providing sufficient confinement for hadronic showers, keeping punch-throughs in the muon system to a minimum. With such a thickness, the hadronic calorimeter provides a good resolution for high energy jets. A good missing transverse energy measurement is also guaranteed due to the large range in η making it particularly useful in SUSY particle searches.

The Tile Calorimeter (TCal) is a sampling calorimeter consisting of one barrel and two extended barrels. The absorbing material is iron and the scintillating tiles are the active material readout by wavelength shifting fibres into two photomultiplier tubes. The signals created by the scintillators are collected and readout via the fibres at a fast rate. The photomultiplier tubes also give a fast rise and transit time of the order of nano-seconds.

The LAr hadronic calorimeters consist of two separate end-caps and one forward calorimeter (FCal). For each endcap there are two individual wheels, comprising of copper plates. The FCAL will face an enormous amount of radiation damage. Its layout is particularly beneficial to the muon spectrometer, acting as a barrier, reducing the levels of background radiation. Consisting of three sections – one copper and two tungsten – each has a metal matrix, with longitudinal channels, regularly spaced and filled with concentric rods and tubes. The tubes and matrix are grounded and the rod held at a positive high voltage. The sensitive medium between the rods and the tube is LAr. As a preventative measure, the FCAL is sunken back with respect to the electromagnetic calorimeter, to reduce the number of back scattered neutrons into the ID cavity.

2.5 Inner Detector

Figure 2.6 shows an image of the ID layout. It is housed within the central solenoid which provides a magnetic field of 2 Tesla to the ID. Momentum and vertex resolution requirements are of key importance throughout the experiment, hence meticulous measurements are needed. A detailed system of different types of detectors are necessary in order to accommodate the large density of tracks anticipated at the LHC. There are three sub-systems associated with the ID: Pixels, Semi-Conductor Tracker (SCT) and the Transition Radiation Tracker (TRT). Cost is an important factor in the decision of which materials to use for each detector type. Silicon micro-strips and pixel detectors within the SCT provide the finest granularity around the vertex region of the experiment. In general, a track passes through 3 pixel layers and 8 silicon strips, equivalent to 4 space points, since there are 2 layers of wafers in a silicon module. At much less cost the TRT provides a vast number of tracking points, in general approximately 36 space points per track. With the combination of all three sub-systems, the resolution in ϕ and z co-ordinates is optimised over the range $\eta \leq 2.5$. Table 2.2 gives a summary of the layout parameters for the ID. Due to the running luminosities of the LHC, the ID is susceptible to a certain amount of radiation, therefore limiting the detector lifetime.

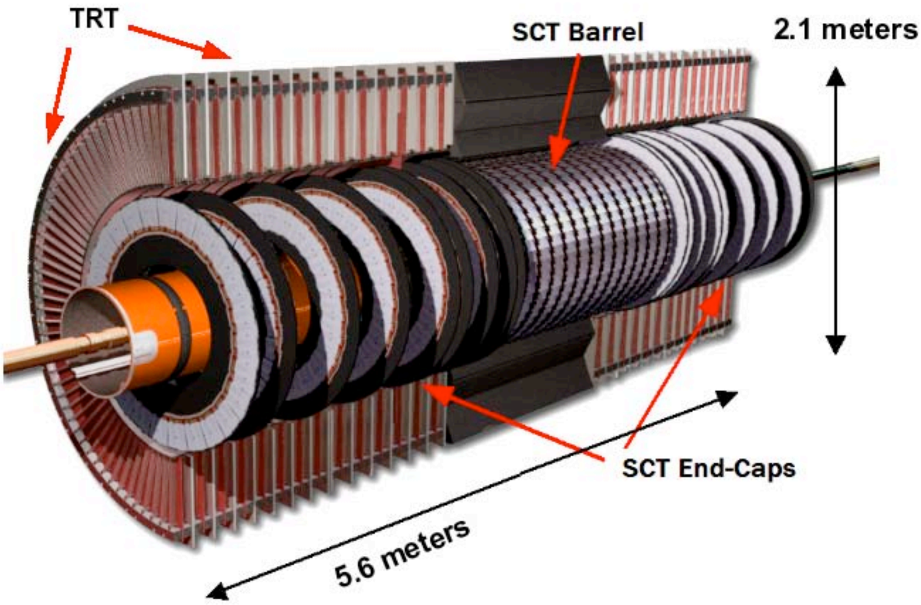


Figure 2.6: Inner Detector.

2.5.1 Requirements

A requirement for the P_T resolution of 500 GeV tracks going through the inner detector is $\frac{\Delta P_T}{P_T} < 30\%$ at $\eta < 2$ and 50 % at η up to 2.5 [11]. The overall resolution can make use of the spacial resolution of all three sub-components of the inner detector. For the pixels,

Table 2.2: Inner Detector parameters.

System	Description	$\|\eta\|$	σ (μm)	Channels (10^6)
Pixels	Layer 0	2.5	$R\phi$ = 12, z = 6	13.2
	Layers 1 - 2	1.7	$R\phi$ = 12, z = 66	54.0
	6 endcap discs	1.7 - 2.5	$R\phi$ = 12, R = 77	13.2
SCT	4 barrel layers	1.4	$R\phi$ = 16, z = 580	3.2
	18 endcap discs	1.4 - 2.5	$R\phi$ = 16, R = 580	3.0
TRT	Axial barrel straws	0.7	130 (per straw)	0.05
	Radial endcap straws	0.7 -2.5	130 (per straw)	0.25

the requirements are 3 space points with a 12 μm resolution and for the TRT it is 36 space points with a resolution of 130 μm. Test beam measurements [17] at CERN show that for non-irradiated modules, a combined spacial resolution of 16 μm in the $R - \Phi$ plane is achieved for the SCT. Even after radiation, the resolution shows no significant degradation.

2.5.2 Pixel Detector

Located at the closest point to the interaction, the high precision pixel detector is comprised of the following: 3 barrel layers segmented in Rϕ and z, placed in concentric cylinders around the beam axis, and 3 endcap discs on either side of the cylinder. The barrels are positioned at radii of approximately 5 cm, 9 cm and 12 cm. The innermost layer was initially designed to be removable but in practice the services preclude this option. Its mechanical design allows the opportunity for replacement, so that the detector performance is not compromised during the high luminosity phase of the LHC. The endcap discs are placed approximately 5 - 6.5 cm perpendicular to the beam axis, and are arranged in planes.

Figure 2.7: The Pixel Detector.

There are 1744 pixel modules equivalent to 80.4×10^6 channels. The design of the pixel modules are identical in both the disc and barrel layers. Each module measures approximately 63 mm in length and 24 mm in width. In order to obtain full hermetic coverage the modules are positioned to overlap in the support structure. With two wafers segmented in both the $R\phi$ and z directions, the readout requires advanced electronics. There are 16 chips per module each with 2880 electronic channels. For every pixel element read out by its corresponding chip, there is buffering provided in order to store data and this therefore results in a large chip area. In order for the chips to survive over 10 years of operation, they must be made radiation hard, capable of withstanding 160 kGy/year of ionising radiation and more than 3 $\times 10^{14}$ neutrons per cm^2.

2.5.3 Semi-Conductor Tracker

The Semi-Conductor Tracker (SCT) is positioned the second closest to the point of interaction, consisting of 4088 modules, with approximately six million readout channels. It comprises 4 central barrels and two end-caps, each with nine discs. The basic element of the system is the module. These as well as the support structure and services were built at the collaborating institutes. The final assembly of the SCT barrel was performed at Oxford, one end-cap was assembled at Liverpool (UK) and the other at Nikhef (Amsterdam). The SCT itself occupies a radial region between 30 and 51 cm. Its design provides 4 space point measurements for a particle originating from the interaction point, up to a pseudo-rapidity coverage of $\eta \geq 2.5$. Figure 2.8 shows the different SCT detector parts.

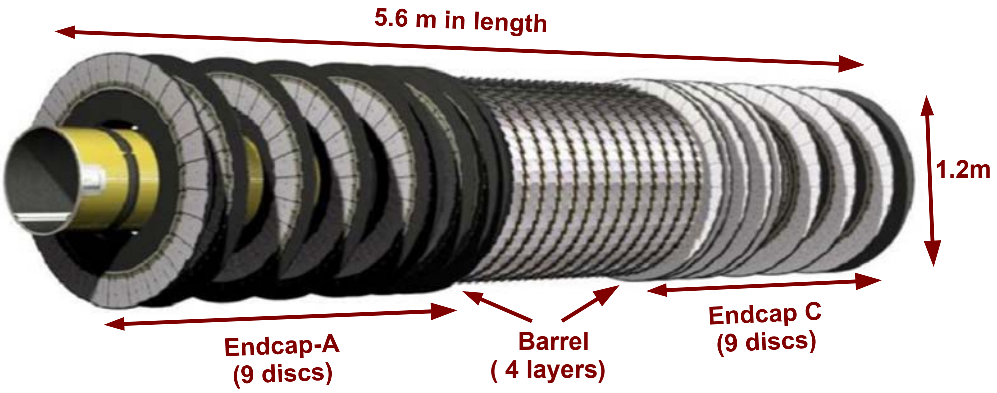


Figure 2.8: The Semi-Conductor Tracker Detector.

In total the SCT has an active silicon area of 61 m^2. Silicon micro-strip technology provides fine granularity, which in turn, aids significantly the momentum, impact parameter and vertex position measurements. Each SCT component (Barrel or Endcap) was transported to CERN for the final support mechanisms and thermal enclosures to be added before being integrated into the TRT and finally installed in the ATLAS detector. Chapters 5 and 6 will describe in detail the assembly and performance of Endcap-A.

The module layout for the barrel and end-cap discs is given in Figure 2.9. In the barrel there is only one module type, however four different types are present in the forward regions. Each module consists of two layers of silicon wafers: one which runs radially and the other offset at a small stereo angle of 40 mrad. The module consists of 4 p-on-n silicon sensors; 2 layers of 2 wafers linked together by wire bonds, giving a readout strip 12.8 cm in length. Each module has 768 readout strips per side with a pitch of 80 μm and a module width of 6.36 cm. The chip electronics are included on the detector itself; consisting of a front-end amplifier and discriminator and a binary pipeline to store the hits. The barrel's four cylinders are placed at differ-

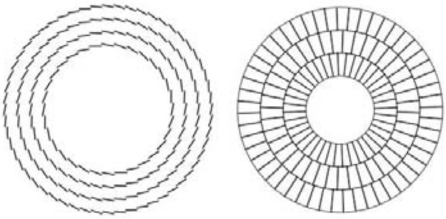


Figure 2.9: On the left is the layout of the barrel modules looking along the direction of the z-axis. On the right is the module layout for one of the fully populated end-cap discs.

ent radii from the beam pipe. There are 12 modules associated to each row of the barrel, which are placed in a tile-like manner and rotated around the axis parallel to the beam pipe. For each endcap, due to the physics requirements of four space point hits up to η = 2.5, combined with the detector volume constraints, this results in a layout consisting of nine discs. The nine discs of each endcap have between one and three rings of modules, – Outer, Middle or Inner – depending on its position. The detector design is constrained by the expected levels of irradiation during the 10 year LHC run. The modules are operated cold (sensors at -7 °C) due to both the heat generated by the front-end electronics and to keep the consequences of radiation damage within limits.

2.5.4 Transition Radiation Tracker

The SCT is surrounded by the Transition Radiation Tracker (TRT). It consists of many small diameter (4 mm) straw detectors, enclosing a single gold-plated sense wire. A radiator material layered between the straws allows the identification of $e^{\pm}$ by means of detecting transition radiation photons. The TRT provides 36 space points per track at very low cost.

The barrel contains 52,544 axial straws of 144 cm in length, at radii between 56 cm and 107 cm. Each straw is split into two equal sections and read-out at both ends. The end-caps contain a total of 245760 radial straws at radii between 64 cm and 103 cm. There are 12 inner radius wheels and 8 outer radius wheels to maintain full acceptance.

In total there are approximately 300,000 electronic channels, each channel providing a drift time measurement of 130 μm spacial resolution per straw and with two different thresholds. These thresholds distinguish between tracking hits at the lower threshold and transition radiation hits at the upper threshold.

CHAPTER 3

SILICON STRIP SENSORS

"The science of today is the technology of tomorrow."

Edward Teller

Contents

The aim of this chapter is to introduce the use of silicon detectors to track charged particles. Then there is a discussion on the damage processes that can occur within the tracking medium. The final part involves a more detailed description of the ATLAS silicon sensors stating the motivation for their design as well as an outline of the individual components of the detector module.

Development of silicon detectors began in 1950 with the first prototype available in 1960. Their first use was in X-ray spectroscopy where a single sensor was used primarily for measuring the energy. In the late 70's a new usage for silicon was established, greatly benefiting from the revolutionary progress in the microelectronics industry. The focus moved away from energy resolution towards using large area silicon wafer processing, enabling the miniaturisation of multiple strips onto one single sensor for the purpose of being position sensitive devices. This led to the combination of sensors with integrated circuits for the readout of each channel. Many parameters were now considered in the performance of detecting charge (not only the energy resolution), including low noise amplifiers, low power consumption and minimal material. The next generation of collider experiments pushed the limits of technology even further with requirements leading to the development of radiation hard processes and faster electronics.

Previously, the electron-positron collider, LEP, at CERN, operated up until the year 2000 where it reached the limit of its energy capabilities at 210 GeV. The HERA machine at DESY in Hamburg Germany, collided 800 GeV protons with 30 GeV electrons, up until its closure in June 2007. At present the Tevatron proton-antiproton ($p\overline{p}$) collider at Fermilab near Chicago is the facility probing for new physics at the energy frontier. The Tevatron is the highest energy collider, with a collision energy of 2 TeV and the ability to produce the very heavy top quark which it discovered in 1995. The LHC due to begin in Summer 2009, will be the world's largest collider, with collision energies of up to 14 TeV. Since also the intensity is unprecedented, the detectors have to withstand extreme radiation conditions. The radiation hard capabilities of silicon allow the use of silicon strip devices for radii greater than 5 cm from the point of collision. High precision, one dimensional co-ordinate measurements are possible using single-sided strip devices with a second co-ordinate available using double-sided devices. Silicon pixel devices are best used in a high track density environment. The active area is much smaller than the strip detectors and therefore allows a high granularity measurement at the expense of a high channel count.

3.1 Silicon Operation Principle

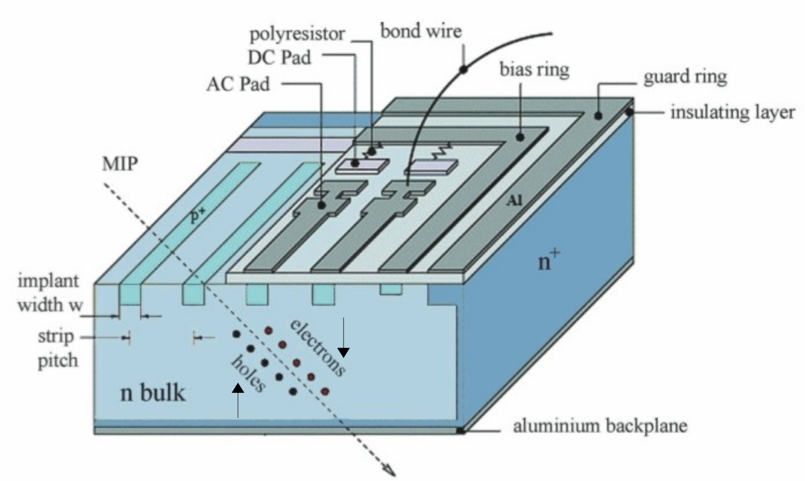


Figure 3.1: A MIP passing through a silicon detector ionising the detector medium and creating electron-hole pairs. The holes are collected by the p^+ strips, inducing a signal on the aluminium read-out strips.

A silicon sensor is a diode (strip) operated in reverse bias with the depleted area acting as the detection volume. Tracking charged particles is one of the main applications in high energy physics. When a charged particle passes through a semi-conductor device, it ionises the material, which in turn creates a so called electron-hole pair. (See Figure 3.1.) The vacant positions left by the electrons within the lattice are known as "holes". They are free to migrate between neighbouring atoms and behave as a positively charged particle. A minimum ionising particle (MIP) passing through 285 μm silicon creates approximately 25,000 electron-hole pairs (eh) equivalent to a charge deposition of about 4 fC within the silicon.

This charge signal is collected on the implant strips and is either direct (DC) or capacitively (AC) coupled to a metal read-out strip. The output is proportional to the induced current pulse in the detector. A good example for further reading on the physics of semiconductor devices can be found in [73].

3.1.1 p-n Junctions

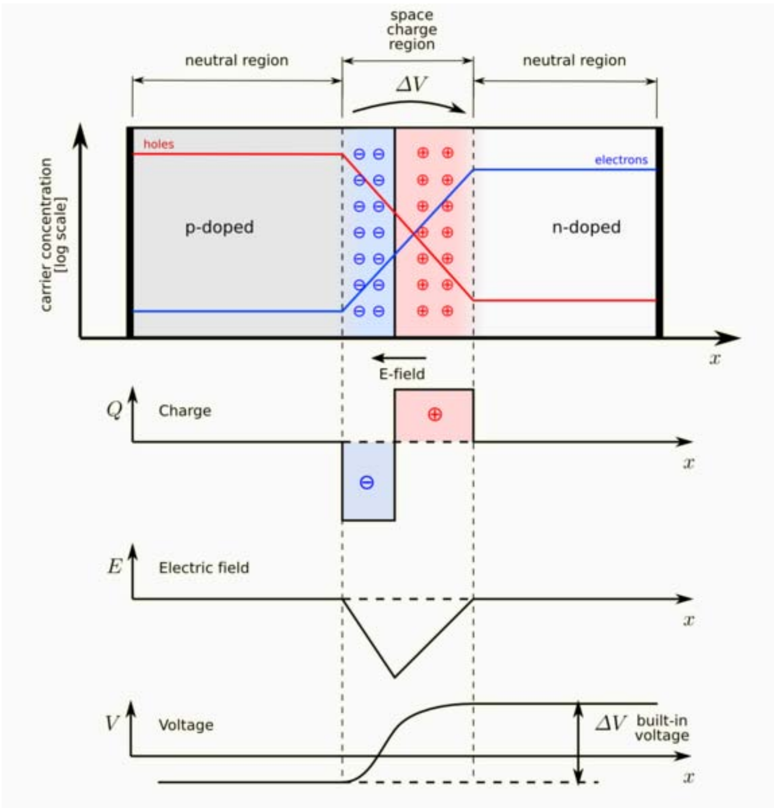


Figure 3.2: Single crystal doped with P and N type impurities develops a potential barrier.

The essential principle of a semi-conductor device is that the conductivity of the material is manipulated by changing impurity concentrations. Doping silicon, for example, with boron or phosphorus, can produce p- or n-type materials with different concentrations of majority carriers. A p-n junction is formed when two such materials are put in contact with each another. When there is no external source applied to a semi-conductor circuit, the separate p and n components maintain the same Fermi level throughout the circuit. The holes diffuse from the p-type material to the n-type material and conversely the electrons from the n-type material diffuse to the p-type material. This creates a depletion of free carriers in an area known as the space charge layer. A negative space charge forms near the p-side of the boundary and a positive space charge forms by the n-side (see Figure 3.2).

The potential difference of this space charge layer generates an electric field. This field is in the opposite direction to the diffusion current for each charge carrier. This creates a potential barrier that stops the current flowing across the junction. When forward biased (p positive with respect to n) this narrows the zone eventually making the junction conductive and allowing free flow of charge carriers. Under reverse bias, the built in potential is increased, resulting in the size of the space charge region growing. This is what is known as the depletion region, with its absence of free carriers. The depletion zone is interesting since any charge within its volume will drift towards its borders (holes to the p-side, electrons to the n-side) as a result of the electrical field. In general a silicon sensor is fully depleted when the depletion width equals the sensor thickness.

Under reverse bias, the current flowing across the depletion region in absence of a real signal, is known as the leakage current. It is usually dominated by thermally generated eh-pairs which move across the junction as a result of the electric field.

3.1.2 Making a Position Sensitive Sensor

A silicon strip detector is designed to detect the number of charge carriers set free by the MIP. The electrons follow the electric field across the detector medium and induce a current. The current is recorded with an amplifier and subsequent electronics. The detection principle works by doping narrow strips of silicon and making them into p-n junctions (diodes), which are then reverse biased. Figures 3.3 and 3.4 show the basic sequence for processing silicon wafers. There are four main steps: oxidation, lithography, ion implantation and metallisation. In this example, the process starts with an n-doped silicon wafer (step 1). There are two SiO_2 growth methods -dry and wet- that can create an oxide layer. This process is called oxidation and takes place at high temperatures, typically between 800-1200 °C (step 2). Step 3 shows the photo-lithography process. A layer of photo-resist is coated on top of the oxide layer and the wafer is heated at $80 - 100$ °C to harden the resist. Next, a mask is used to define the pattern needed on the wafer. Using ultra-violet light the wafer is exposed through the mask pattern. In this case a negative resist was used, with the area exposed to light forming a window in the oxide layer. The entire wafer is then put into a developer and the unexposed resist region washed away. The etching process removes the unprotected area of silicon oxide.

Step 4 shows the method of ion implantation or diffusion. Localised regions of p^+ implant are built up on the wafer by subjecting the exposed silicon region to a high concentration of p-type (boron) impurity atoms. On the back side, phosphorus atoms build up an N^+ layer at the back-plane. The final region of p^+ is wider than the initial window (step 5). Next the entire wafer is annealed at approximately 600 °C before the final step (6) when ohmic contacts are formed via metallisation.

3.2 Silicon Micro-strip Sensors

The inner detector of ATLAS consists of silicon pixels, silicon strips and a straw-tube tracker. The silicon strip detector is built from one similar sensor type (albeit with some variation in outer shape and size). The sensors were fabricated on <111> orientated silicon. Each sensor uses an n-type high resistivity bulk with a p^+ type implant. The strips are AC-coupled. The barrel read-out strips all have the same pitch of 80 μm, whereas due to the different end-cap geometries, their strip pitches vary between 56.9 an 94.2 μm. Despite the different geometries, both barrel and end-cap sensors have the same active surface area (to within 6%), except for the W21 wafer (inner) which covers only 76% of the nominal area. Table 3.1 shows the wafer types for both barrel and end-cap modules as well as their corresponding geometric dimensions. Two manufacturers, Hamamatsu [43] and CiS [25] produced the sensors (see Figure 3.5). There are differences between the two, as a result

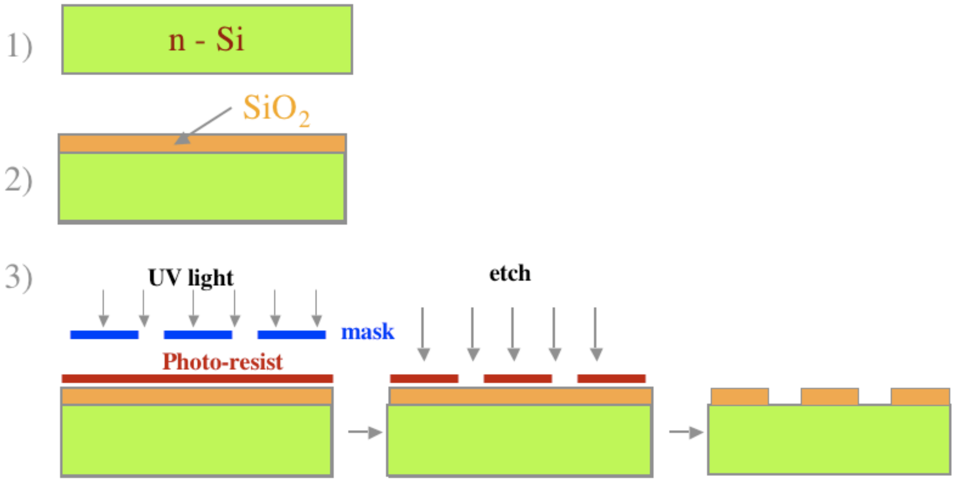


Figure 3.3: The oxide growth and photo-lithography stages in wafer processing.

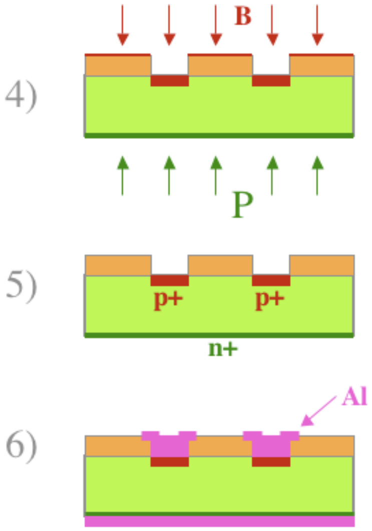
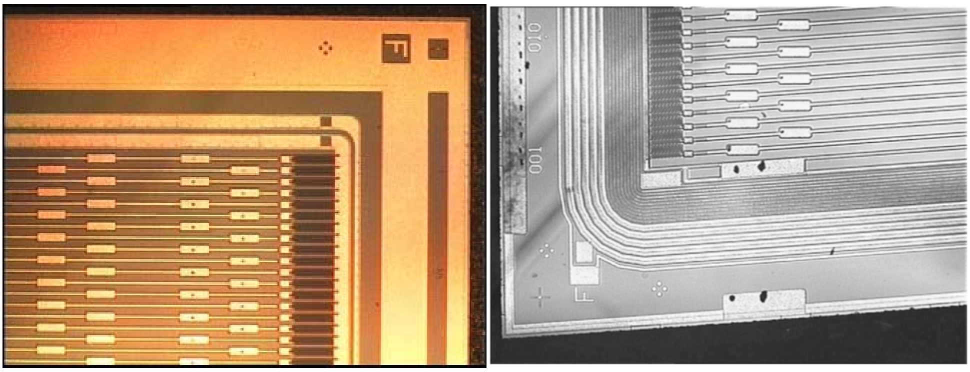


Figure 3.4: The ion implantation/diffusion process followed by the final metallisation layer. The end result is a sensor with several p-n junctions used for particle tracking.



(a) (b)

Figure 3.5: A close up of the two different wafer designs. (a) is a Hamamatsu wafer with a single floating guard, and (b) is the CiS wafer, multiple guard structure.

Table 3.1: Cut values of the silicon wafers. The barrel modules have their strips aligned parallel to one another whereas the end-cap strips run radially to one another. The strip-strip angle is the angle between the neighbouring strips

Module	Sensor	length	$\text{Width}_{\text{out}}$	$\text{Width}_{\text{inn}}$	Strip pitch	strip-strip angle
		(mm)	(mm)	mm	(μm)	(μrad)
Barrel:	Barrel	63.960	63.560	63.560	80.0	0
End-cap:						
Inner	W12	61.060	55.488	45.735	56.9-69.2	207.0
Middle	W21	65.085	66.130	55.734	69.9-83.0	207.0
(Short) midd	W22	54.435	74.847	66.152	83.4-94.2	207.0
Outer	W31	65.540	64.635	56.475	70.9-81.1	161.5
Outer	W32	57.515	71.814	64.653	81.5-90.4	161.5

of the processing methods both manufacturers use. The SCT group gave a common design specification, leaving small design details to be optimised by each manufacturer. Hamamatsu produced all of the barrel sensors and 82.8 % of the installed end-cap sensors. The remainder were produced by CiS, forming the middle/inner module types. The current-voltage (I-V) scans of the sensors during module production showed a clear moisture dependence in different environments. As a result of the field plate geometry, the CiS sensors behaved differently in a dry environment. The Hamamatsu design adopted an overhanging metal electrode which limited the breakdown risks in the high-voltage biased detectors. An explanation for the differing behaviours follows (for full details see [45]).

When there is no external bias voltage, an electron accumulation layer develops in the conductive silicon bulk. It is induced by the positive charge in the SiO_2 layer of the inter-strip region. Let us first consider two separate environment situations: moist and dry. In a moist environment, as the bias voltage is applied, the positive charge on the back plane induces a negative counter charge on the detector surface around the edge of the p^+ implanted strips. The positive charge in the SiO_2 layer is reduced until finally the accumulation layer is completely emptied and the full silicon bulk gets depleted. However, for this process to take place the inter-strip surface has to be conductive, enabling removal of the excess positive charge.

In a dry environment, the surface is non-conductive and becomes positively charged by induction. The charge in the SiO_2 is only partially emptied, leaving a stubborn undepleted zone in the inter-strip region. Figures 3.6 and 3.7 show the different depletion behaviour in the moist and dry environment. This results in an increased inter-strip capacitance. Due to small geometry variations, this has different implications for the sensors manufactured by Hamamatsu and CiS. It is expected that these differences will disappear after mild irradiation since the oxide itself will become charged.

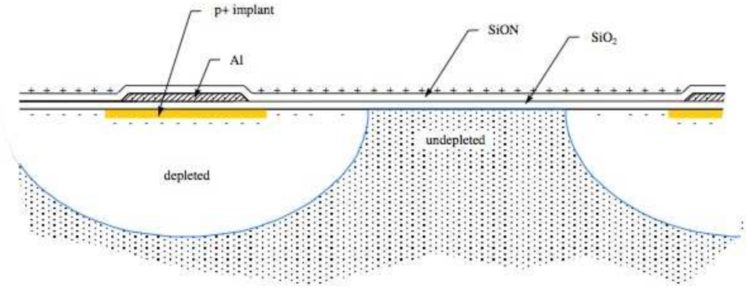


Figure 3.6: Inter-strip depletion region in a dry atmosphere [45].

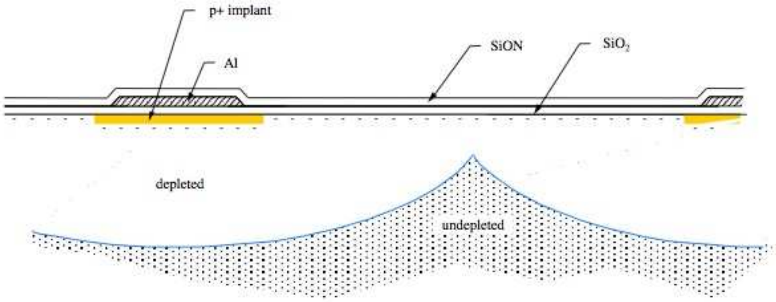


Figure 3.7: Inter-strip depletion region in a moist atmosphere [45].

Hamamatsu

The p-in-n strips are biased via a poly-silicon resistor. The sensor design uses a field plate geometry whereby the metal readout strip (22 μm) is wider than the implant strip (16 μm). Silicon-nitride and Silicon-oxide layers insulate the metal strips from the implant. This field plate geometry delays the onset of strip micro-discharge when the bias voltage is ramped in a dry environment. Actually the metal strips shield the implant from the high potential, caused by the positive voltage applied to the back-plane. This shielding effect also reduces the inter-strip capacitance for this geometry type. Figure 3.8 shows this shielding effect using the field-plate geometry. A single floating guard ring with an extended aluminium electrode defines the edge of the sensor. The whole of the front-side of the sensor and the metal read-out strips are covered by a passivation layer of SiO_2.

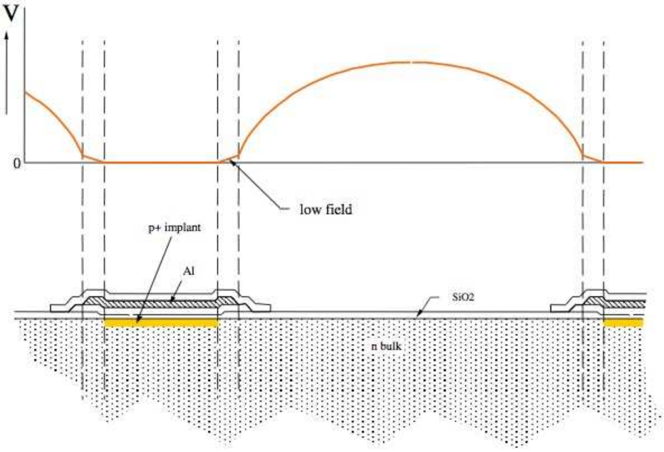


Figure 3.8: Hamamatsu sensor using a field plate geometry. The metal strip shields the implant from a high potential field in the inter-strip region [45].

CiS

These sensors show moisture sensitivity as a result of the geometry design. The sensor uses a non-field plate technology where the metal read-out strips are narrower than the p^+ implants by 4 μm. This design has consequences since the majority of un-irradiated CiS sensors have a problematic strip micro-discharge when placed in a dry atmosphere. Figure 3.9 shows the non-field plate geometry used in the CiS design. Studies of the CiS sensors show a clear moisture dependence in the behaviour of the sensor current-voltage scans. In a wet environment (RH = 40 - 50 %), the I-V curves were good. However, in a dry environment, the results show a breakdown of charge, at the edge of the p^+ implants. Due to the metal strip being narrower than the p^+ implants, the high inter-strip capacitance region has a direct impact on the I-V behaviour of the sensor. Since it is not shielded by the

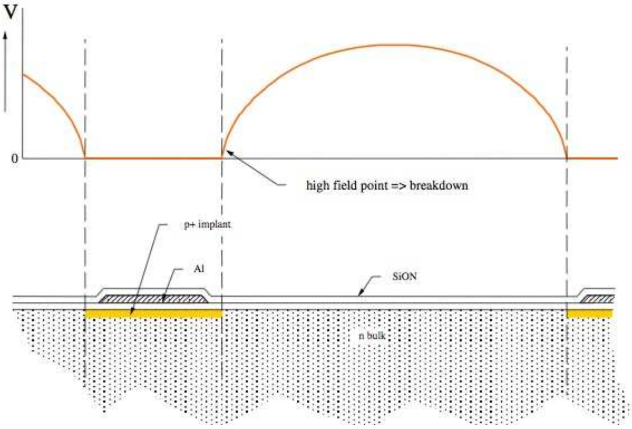


Figure 3.9: CiS sensor with the non-field plate geometry. Here a high potential field exists in the inter-strip region [45].

metal strip, the strip micro-discharge takes effect early on in the I-V scan. Fortunately, this effect could be easily controlled, by training the sensor. This meant, changing from a wet environment to a dry one whilst biasing the sensor at 150 V. However, since the implanted p^+ strips are open to such high fields, the inter-strip capacitance for this module geometry is higher than for that of the field-plate geometry.

The next sections highlight the motivation for the design of the SCT module and the specifications set out by ATLAS, in order to deliver the required physics performance. A more in depth description is given of the construction of the silicon detector module, including a short overview of it's individual components.

3.3 Module Design and Operation

There are 4088 modules, equating to 15392 silicon strip wafers in the SCT. The barrel section has 2112 modules with only one module type, whilst each end-cap has nine discs populated with trapezoidal modules[1]. Figure 3.10 shows the main components that make up a module. A detector module consists of gluing two pairs of single sided sensors, back to back on a highly thermally conducting substrate. There is a small stereo angle of 40 mrad between each side. Figure 3.11 shows a typical module of each type for the end-cap discs. Each of these sensors is approximately 6 cm long, giving 12 cm for the barrel modules as well as the outer and middle end-cap modules. The short middles and inners are only 6 cm. Each sensor is read out by Application Specific Integrated Circuits, known as ASIC chips. Each module side is served by 6 of these chips, each one responsible for 128 read-out channels, giving a total of 1536 channels per module. Optical communication fibres exist for both sides of the module to be able to send/receive data to/from each detector. Chapter 4 will go into more detail on the module read-out components and architecture.

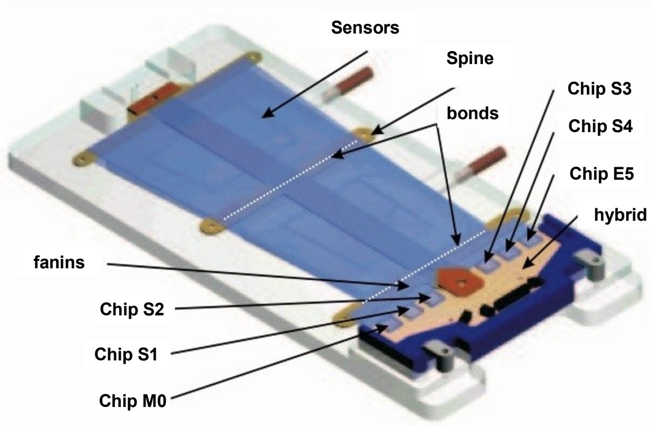


Figure 3.10: The components which comprise one module. Here an endcap outer module is shown.

Figures 3.12 and 3.13 show the layout of the p-n-n^+ micro-strip detectors in both transverse and longitudinal views. The highly-doped n^+ layer is in contact with the detector

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[1] Each end-cap has four module types –Outer, Short Middle, Middle and Inner– containing a combination of five wafer types:W12, W21, W22, W31 and W32. The inner modules use only the W12 wafer types, whereas the short middles are constructed using a pair of W22 wafers. The normal middles consist of two pairs of W21 and W22 wafers, and finally the outer modules use two W31 wafers and their corresponding partner set of W32 wafers.

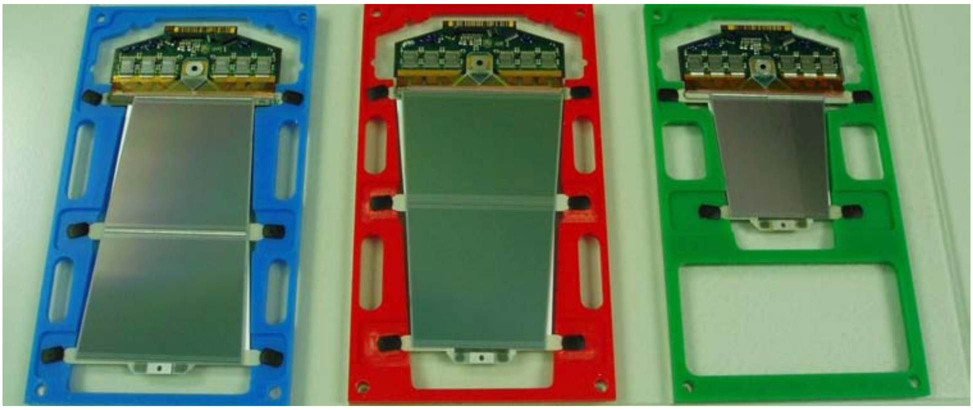


Figure 3.11: Three of the SCT module types. From left to right:An Outer, Middle and Inner module. A short middle consists of a pair W22 wafers, corresponding to the upper wafers as seen in the middle figure.

back-plane. The nominal operation is +150 V and is connected via the spine and conducting glue to the backplane. The guard ring is an additional p-n junction that acts as a barrier isolating the main junction from the edge of the sensor, protecting it against premature high-voltage breakdown. All of the Al strips are connected to the bias ring by either polysilicon or implanted meander bias resistors so that all of the strips share a common potential, but are insulated. In our case the bias ring is connected to ground to prevent a large potential difference between the strip and the amplifier. The p-implants are AC coupled to the metal read-out strips.

Under the action of this created electric field, the electrons drift towards the positive electrode at the back-plane and the generated holes move towards the more negative potential of the p^+ implants (grounded). During their drift, electrons and holes are diffused by multiple collisions. Due to the motion of carriers, signals will be induced on the electrodes. The current induced by a moving carrier on an electrode can be evaluated by applying the Shockley-Ramo theorem, and taking into account the drift velocity and the weighting field [72]. Data from the test beam, shows that the majority of the charge is deposited in one strip, with charge shared between neighbouring strips accounting for only 10% [58]. The hole-induced current is then fed and amplified by the front-end read-out electronics.

3.3.1 Specifications

It is extremely important that the charge is efficiently collected at the amplifier input. Subsequently, the threshold must be adjusted such that the noise is kept to a minimum, whilst the efficiency is maximised. The maximum allowed noise during the initial LHC start-up is 1500 ENC, increasing to 2000 ENC during the end of the detector lifetime. Figure 3.14 shows the typical occupancy distribution at a given threshold, for a MIP particle depositing approximately 3 fC of charge in the detector. Noise (dotted line) has an approximately Gaussian distribution. The actual charge seen by the discriminator of the module channel, due to the MIP charge is a Landau distribution convolved with the Gaussian noise. This is called an improved Landau distribution, given by the pale black line in the figure. By setting the discriminating threshold of a channel above the noise level, the efficiency can be maximised (thick black line). If this threshold is then varied there are effects on both

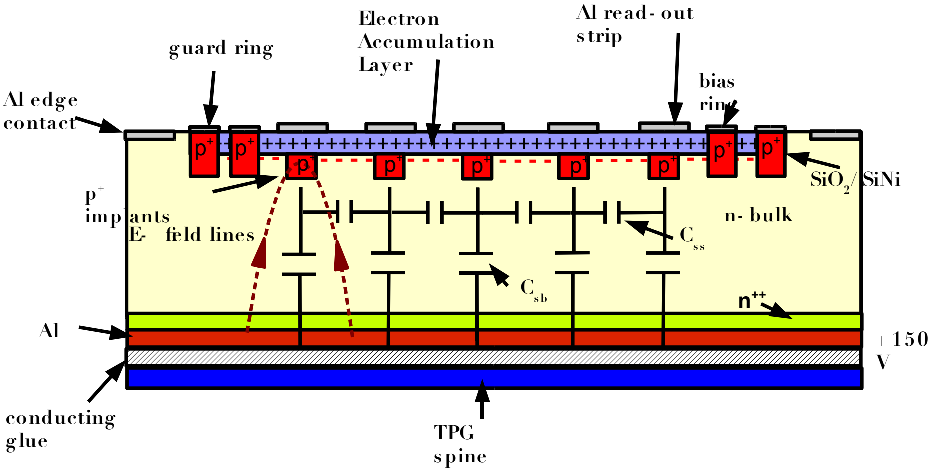


Figure 3.12: Transverse view of the SCT silicon sensor.

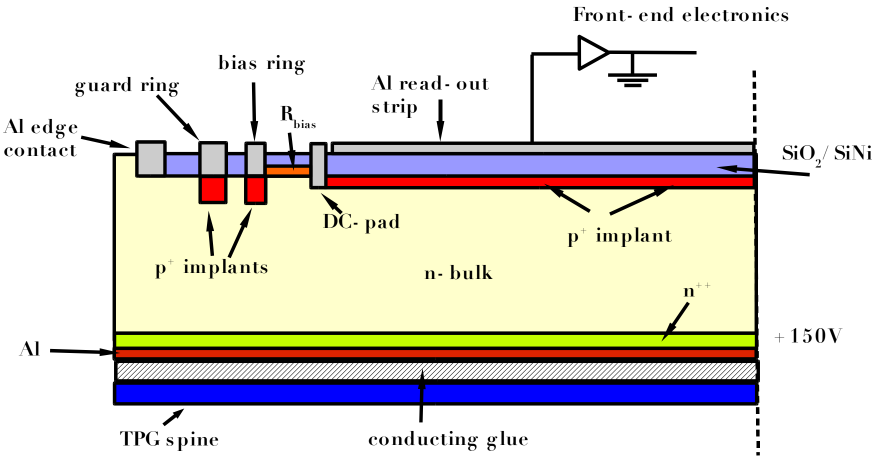


Figure 3.13: Longitudinal view of the SCT silicon sensor.

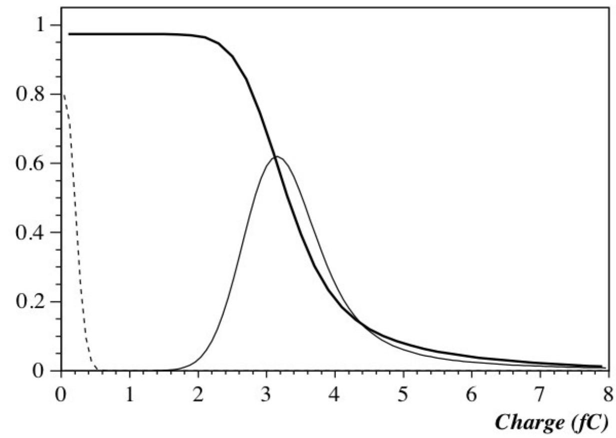


Figure 3.14: An improved Landau distribution (pale black line), noise distribution (dashed line) and the efficiency versus threshold (thick black line) for a typical silicon detector [62].

efficiency and noise. A very fine balance between the two results in a nominal threshold setting of 1 fC, which corresponds to ≈6250 ENC. With these specifications in place, this gives an efficiency better than 99% and a noise occupancy less than 5×10^{-4}.

The tracking resolution is defined by the strip pitch, P. In the case of the barrel where the pitch is 80 μm, the sensor strip resolution is computed in the following way:

$$\sigma_{strip} = \sqrt{\bar{x^2} - \bar{x}^2} = \sqrt{\frac{1}{P}\int_{\frac{-P}{2}}^{\frac{+P}{2}} x^2 dx} = \frac{P}{\sqrt{12}} \tag{3.1}$$

$$\sigma_{strip} = \frac{80}{\sqrt{12}} \approx 23\ \mu m. \tag{3.2}$$

Since the detector modules consist of two sensors glued back to back with a stereo angle of 40 mrad between them, the overlapping strips from the front and back side give respectively an r-ϕ and z resolution:

$$\sigma_{r-\Phi} = \frac{\sigma_{strip}}{\sqrt{2}} \approx 16\ \mu m. \tag{3.3}$$

$$\sigma_z = \frac{\sigma_{strip}}{\sqrt{2} sin(20 mrad)} \approx 907\ \mu m \tag{3.4}$$

$$\sigma_z(2 \text{ SCT layers}) = \frac{907}{\sqrt{2}} \approx 640\ \mu m. \tag{3.5}$$

For the case of the end-caps, the pitch varies depending on the sensor type, but the resolutions are comparable to the barrel.

Another specification is that the signal to noise ratio is better than 15 at the LHC start-up degrading to 10 at the end of the detector lifetime. It is also a requirement that all of the channels in a chip respond in the same manner to charge that is deposited. Otherwise, this will induce biases in the detector tracking algorithms using extra or missing hits. To ensure that this does not occur, an internal charge injection calibration exists, which will be described in detail in the next chapter.

Finally, during the module production, a limit of 1% of the module channels are allowed to be defective (corresponding to 15 channels). Defects range from scratches in the Al strip to shorted strips, to pin holes, to broken strips and missing bonds. In the case of a scratch, an upper limit of 7 consecutive channels is put in place. For a good overview of the causes of bad channels see [32].

Table 3.2 gives an overview of the principle parameter requirements, including mechanical, electrical and thermal tolerances. For more specific information, please refer to references [6], [1], [3].

3.3.2 Module components

Each module type, either barrel or end-cap, share the same conceptual design. In the next paragraphs a description of the end-cap module components is summarised.

3.3.2.1 Spine

The spine provides the support for the silicon wafers that are glued back to back. It is made from 500 μm thick thermalised pyrolytic graphite (TPG), a vital material responsible for the transportation of heat away from the silicon sensors. It is covered with a layer of Parcylene-C to keep the TPG electrically insulated and mechanically preserved. At each end of the spine, it’s contacts coincide with module cooling blocks. The TPG itself is extremely delicate and therefore is strengthened using Aluminium Nitride (AlN) ceramic additions. As a result of the temperature changes that the SCT module will be subjected to, AlN was chosen due to its high level of thermal conductivity (180 W/mK at 20 °C). At each end of the spine, AlN support sections are placed to provide a good interface to the cooling blocks. Two additional central wings are also positioned to provide extra support to the silicon wafers. The bias voltage necessary to bias the silicon sensors is propagated via metal traces. These are contained within the AlN supports at both the hybrid and central support wings. Since the bias voltage is only supplied to one side of the spine, but needed on both, a metallised through hole is created, electrically connecting the two spinal sides.

3.3.2.2 Fan-ins

Due to the complex design of the SCT module, a pitch adapter is needed to enable the wire bonding connection between the chips and the sensors. For the end-cap (barrel) the pitch of the chips input pads is 96 μm (40 μm) compared to the varying output pad pitches of the sensors. They range between 140 μm and 190 μm depending on which module type (80 μm for the barrel). There are 768 strips to be connected on each module side. Each chip is responsible for the read-out of 128 channels. The function of a fan-in is to act as an adapter between the different pitches, electrically connecting each channel to its corresponding chip. It also provides a mechanical support between the hybrid and the sensors as well as an acting heat barrier at this hybrid-sensor junction. For each module, four fan-ins are required, one for every three read-out chips. Each fan-in consists of an isolating glass substrate implanted with 384 high density metal traces. The traces are an aluminium/copper mix (99.5 % / 0.5 %), with each trace protected via a passivation layer.

Parameter	Description
Number of strips	2 × 768 active strips
Strip rotation	± 40 mrad
Nominal resolution	16 μm (R-Φ), 907 μm (z or R)
Module dimensions:	
-barrel	126.09 (+2.09) mm
-outer end-cap	119.4 (+2.09) mm
-middle end-cap	115.61 (+2.09) mm
-inner end-cap	63.58 (+2.09) mm
Specified build tolerance (RMS accuracy)	
Barrel back-to-back in plane	< 8 μm (± 2.1 μm) (lateral)
	< 20 μm ± 2.7 μm (longitudinal)
End-cap back-to-back in plane	< 5 μm (± 1.6 μm) (lateral)
	< 10 μm (± 1.3 μm) (longitudinal)
End-cap envelope:	< 115 μm (± 20 μm)
Barrel fixation points	< 40 μm (± 10 μm)
End-cap fixation points	< 20 μm (± 6 μm)
Operating silicon temp	-7°C (average)
Uniformity of silicon temp	< 5 °C
Hybrid power	5.5 - 7.5 W
Sensor bias voltage	Up to 460 V bias on detector
Sensor power	< 1 W at -7 °C

Table 3.2: SCT module specifications-some principle parameters of the produced modules. For the module dimensions the number in brackets represents the dead space between the sensors. In the rows giving the specified build tolerance the numbers quoted in brackets are for the actual build accuracy.

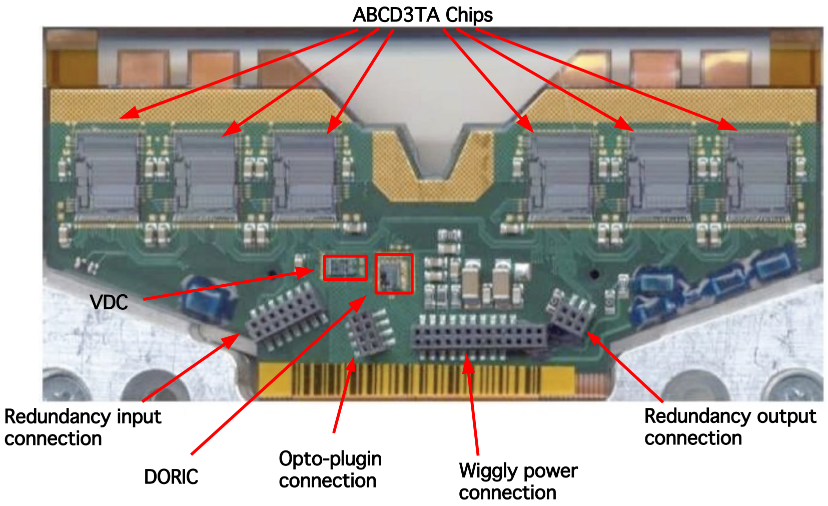


Figure 3.15: A photograph of the front of an end-cap hybrid.

3.3.2.3 Hybrid

The hybrid consists of a multi-layer copper kapton flexible design, folded around a carbon-carbon substrate. For the barrel module, it is folded around the central part of the module between the two sensors on the front and back sides, and for the end-caps (see Figure 3.15) it is folded along the edge of the detector. Its body thickness is 279 μm and 149 μm at the wrap around. There are two sides to the hybrid which act, to some extent, independently from each other, commonly named, Link 0 and Link 1. Each side has six ABCD3TA read-out chips, with the front side of the hybrid having two extra chips to provide the optical communication. There are six layers of copper/polyimide, two which are used solely for analogue ground and power to the module. The carbon-carbon substrate has a low mass and high thermal conductivity. The substrate makes direct contact with the module cooling blocks and provides a thermal path for the heat from the chips to flow away. Each chip is glued onto the flex using Eotite P102, an electrically conductive silver epoxy. A small recess is cut into the flex, and filled with AlN, to improve the thermal path for the chips.

The next chapter will give a description of the front-end electronics, explaining in more detail the ABCD3TA read-out chips and the associated components from the front-end. Before this, however, a short review of radiation damage in silicon and its associated induced defects will be given, relevant for the remainder of work in this thesis.

3.4 Radiation Effects in Silicon

Every 25 ns at the LHC a proton-proton interaction will occur, with a centre of mass energy of 14 TeV. Located as close as a radius of 30 cm from the interaction point, the SCT will suffer from a harsh radiation environment. At full luminosity, the modules will be subject to a neutron equivalent radiation flux of approximately 2×10^{14} cm^{-2} each operational year. This will be detrimental to the lifetime and performance of the detector. The following sections will describe the different radiation effects possible in silicon as well as the impacts that these have on the detector performance.

3.4.1 Particle Interactions with Matter

Heavy charged particles, such as alpha particles, protons and muons pass through a block of material by interacting electromagnetically with the electrons (and to a much lesser extent, the nuclei) in that material. The charged particle provides an impulse to the atomic electrons as it passes them, resulting in ionisation energy losses as well as emitting radiation leading to radiation energy losses. The charged particle undergoes many interactions in its passage through the material, the strength of each depending upon how close the particle came to a given electron. Therefore this energy loss is a statistical process.

3.4.1.1 Energy Loss of a Charged Particle

The Bethe-Bloch formula describes the mean rate of energy loss per unit length for a charged particle in an absorbing medium. The equation takes into consideration the properties of the material in question, for example, it's atomic number and mass.

$$\frac{dE}{\rho dx} = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} [\frac{1}{2} ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta \beta \gamma}{2}]$$

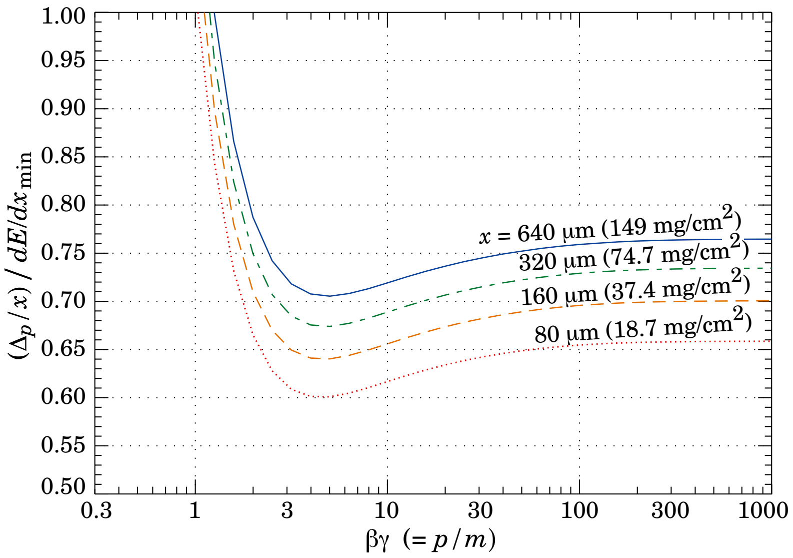


Figure 3.16: Most probable energy loss in silicon, scaled to the mean loss of a minimum ionizing particle, 388 eV/µm (1.66 MeV $g^{-1}cm^2$) [64].

Whereby K is the constant $4\pi N_A r_e^2 m_e c^2$, and m_e, r_e, c, N_A are standard constants as listed respectively: the electron mass, the classical electron radius, the speed of light and Avogadro's number. Z, A and ρ are the atomic number, atomic mass and the mass density of the propagating material. $\beta = \frac{v}{c}$ and gives the speed of the incident particle, γ is the Lorentz factor and z is the charge of the incident particle. Finally, T_{max} is the maximum energy lost by the charged particle in any collision with the atomic electron; I is the mean ionisation potential, meaning the average energy a particle loses by an interaction with an electron; δ is a correction factor. Statistical fluctuations can be quite significant, especially in thin layers of material. These fluctuations are asymmetric and are described by the Landau function, which has a long tail towards higher energies.

Figure 3.16 shows that slower moving particles lose energy more quickly. This can be interpreted as particles having more time to interact. For slow particles the mean energy loss per unit length goes as $1/\beta^2$, while for high energy particles, β is essentially a constant and the rate rises logarithmically, as the relativistic effects begin to dominate. The minimum lies between $\beta\gamma$ = 3 and 4. Particles around this minimum are named minimum ionising particles or MIPs. This minimum is the point at which the particle minimally excites the material. A MIP loses 1-2 MeV for each $\mathrm{g/cm^2}$ of material traversed. The rise after this point is known as the relativistic rise and eventually reaches saturation at the Fermi plateau.

3.4.2 Radiation Damage

Radiation damage to silicon detectors occurs in two ways; bulk damage and surface damage.

1. **Bulk Damage** When an incident particle has sufficient energy ($\approx$ 25 MeV) and collides with a silicon atom (known as a primary knock on atom,) it can displace it from its position in the lattice. This produces an interstitial silicon atom and a vacancy, known as a Frenkel pair. The creation of a Frenkel pair in the crystal lattice is the first process to cause damage in the bulk. If there is enough energy the silicon atom

is able to create more and more defects in a process referred to as cascading. As the atom moves along its path it loses energy, finally coming to a halt, resulting in a region known as a cluster. At temperatures above 150 K these primary defects are then mobile within the silicon bulk due to a diffusion process. They can combine with point defects, inducing irreversible damage to detector properties. These defects can generate higher leakage currents and change the effective doping concentration which leads to a modification of the full depletion voltage. The charge collection efficiency is also lowered, since the electrons or holes, created by the ionisation particle, become trapped.

2. **Surface Damage** Surface damage is determined mostly by the design of the detector and can lead to trapped charges in the oxide layers. Both the the passivation layer and coupling oxide are composed of SiO_2. The passivation layer which forms the surface of the silicon detector, has a net positive charge, which although kept to a minimum during the manufacturing process, is not quite capable of being fully eliminated. The incident particle traversing the surface can create eh-pairs in the SiO_2. Without an electric field, these pairs would recombine, however in an AC coupled device this is not the case. This capacitor has an electric field which separates the opposite charged particles in the oxide. This causes the electrons to be extracted from the layer and injected into the bulk, leaving an increase in the oxide positive charge. These positive charges cause a build up of electrons in the bulk of the detector close to the Si/SiO_2 junction, whilst the holes can stay trapped at this interface. The positive charges in the oxide attract the free electrons carriers in the bulk, modifying the electric field in the inter-strip region, resulting in an increase in the inter-strip capacitance.

The scaling hypothesis makes it possible to compare the amount of radiation damage induced by different particles at different energies. According to NIEL scaling (Non-Ionising Energy Loss), any particle fluence can be reduced to an equivalent 1 MeV neutron fluence producing the same bulk damage in a specific semiconductor. The hypothesis assumes that the bulk displacement damage is linearly dependant on the non-ionising energy transfers to the lattice. Given any particle fluence Φ_1 the 1 MeV equivalent fluence Φ_{eq} is

$$\Phi_{eq} = \kappa \Phi_1$$

where κ is called the hardness parameter and depends on the particle type and energy.

3.4.3 Impact of Radiation on Detector Performance

Ionisation damage is quantified in terms of the amount of energy absorbed per unit mass of the material (1 Gy = 1 J/kg). Displacement damage fluences are all normalised to the equivalent fluence of 1 MeV neutrons (F_{neq}) under the assumption of the NIEL scaling hypothesis. There are three sources to consider in the inner detector radiation environment:

- Primary particles produced in the proton-proton collision;
- Secondary particles interacting with the beam pipe and materials of the ID;
- Albedo neutrons caused by neutrons back-splashing from hadron cascades in the calorimeters.

The radiation requirements of the SCT detector, assuming a 10 year duration of running, is that it can withstand a particle fluence of 2×10^{14} 1 MeV neutron equivalent cm^{-2} and a

1×10^5 Gy/yr ionising dose. Using the predictions from FLUKA transport code [13], an estimate for the particle fluences and doses is calculated. The values predicted assume that there are three years of low luminosity running and seven years at high luminosity.

Radiation damage affects several macroscopic parameters, deteriorating the performance of the detector. These are:

- Increase in leakage current;
- Loss in charge collection efficiency;
- Change in the effective impurity concentration;
- Increase in inter-strip capacitance.

3.4.3.1 Leakage Current

Even in an ideal diode, the thermally induced current is not negligible. In reality the silicon can have impurities, contaminations and process-induced defects. The induced radiation which causes the leakage current is made up of two different parts: Bulk-generation current and Surface-generation current. The bulk current is caused by deep levels that are formed by defects, allowing electrons to be promoted to the conduction band and at the same time, holes to be released to the valance band. This process creates a so called intermediate step between the two energy bands. It is seen as a source for free charge carriers in the space charge region and can lead to an increase in the leakage current. The surface generation is a result of the $SiO_2 - Si$ interface states. However, for neutron irradiations that the SCT will primarily be subjected to, the surface current is not important.

The radiation induced reverse current is proportional to the particle fluence and to the particle and energy dependant damage coefficient α.

$$I = I_0 + \alpha \cdot \Phi \cdot V \cdot \tag{3.6}$$

where I_0 is the leakage current before irradiation and V is the detector volume. Furthermore, the bulk generation current is strongly temperature dependant. It is given by:

$$\frac{I_2(T_2)}{I_1(T_1)} = \left(\frac{T_2}{T_1}\right)^2 exp\left(-\frac{E_g}{2k_B}\frac{(T_1 - T_2)}{T_1 \cdot T_2}\right), \tag{3.7}$$

where I is the leakage current, T is the temperature, k_B is Boltzmann's constant and E_g is the band gap energy.

3.4.3.2 Charge Collection Efficiency

The second effect results in a decrease in the amount of charge collected. This is due to radiation induced defects that act as traps. An electron/hole pair can be trapped for a short period of time, resulting in a reduced number of carriers $N_{e,h}$ collected at t_c, the collection time of the readout electronics. There is an exponential decrease in the number of electron/hole pairs, described by:

$$N_{e,h}(t_c) = N_{e,h}(0) \cdot exp\left(-\frac{t_c}{\tau_{eff}}\right), \tag{3.8}$$

where $N_{e,h}(0)$ is the initial number of charge carriers and $\frac{1}{\tau_{eff}}$ is the effective trapping probability.

3.4.3.3 Effective Impurity Concentration - Depletion Voltage

One of the most damaging effects due to radiation is an increase in the full depletion voltage. The depletion voltage, V_{dep} is proportional to the effective doping concentration N_{eff} (the difference between the number of ionised donors and acceptors in the depletion region). It's relationship is given by:

$$V_{dep} \approx \frac{q_0}{2\epsilon\epsilon_0}|N_{eff}|d^2, \tag{3.9}$$

where q_0 is the charge of the electron, *d* is the detector thickness and ϵ is the permittivity of silicon.

In the majority of silicon detectors, the bulk material is slightly n-doped. Normally, the donor states transfer electrons to the conduction band. However, in the presence of a defect, donor states are removed and acceptor states created. The explanation for this is that the defects become charged by capturing charge carriers. This fixed charge compensates for the positive charge of the donor levels.

This leads to a change in the space charge region from positive to negative. Essentially the silicon bulk changes from being n-doped to p-doped. For n-type silicon, donor removal occurs, with the number of donors decaying exponentially as a function of the fluence. The doping concentration continues to fall until eventually the number of acceptor states equals the number of donor states. The material at this point is said to be intrinsic. With increasing fluence, the effective dopant concentration begins to rise again, however, this time the material is more p-type. This process is referred to as type inversion and causes the full depletion voltage to increase, as seen in Figure 3.17. If the voltage needed to deplete the silicon is higher than the operational voltage of the detector, then the silicon will only be partially depleted. In the case of the SCT detectors, this results in a complete loss in signal and the detector modules would be unusable.

3.4.3.4 Radiation Damage Annealing

In irradiated silicon, the effective doping concentration is not constant, but temperature and time dependant. The changes in the concentration of an irradiated detector, can be separated into three different components and can be parametrised as:

$$\Delta N_{eff}(\Phi, t(T_a)) = N_A(\Phi, t(T_a)) + N_c(\Phi) + N_y(\Phi, t(T_a)), \tag{3.10}$$

where Φ is the particle fluence and T_a is the annealing temperature. Annealing is the reordering of defects within the silicon lattice due to heat treatment. The annealing curve, shown in Figure 3.18 gives the changes in effective doping concentration as a function of time.

N_A has a somewhat short time constant and is referred to as *short term annealing*. After a type inversion, the depletion voltage is seen to decrease and as a result this process is called *beneficial annealing*. The stable component, N_c, describes defects which are stable at temperatures up to 100°C. It has no time dependence and cannot be controlled by a choice in temperature. The last part of the annealing process is a phenomenon denoted as *reverse annealing,*N_Y. It differs from the beneficial process, since it results in the rise of the effective acceptor concentration, causing an increase in the depletion voltage. It also has a much longer time constant ($\approx$ 500 days at room temperature). The number of acceptors activated in this process is proportional to the 1 MeV neutron equivalent fluence Φ. The SCT sensors are kept under cold conditions to prevent reverse annealing.

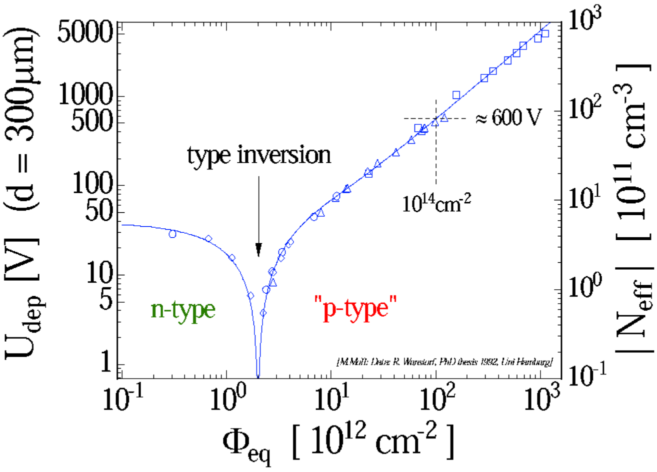


Figure 3.17: *The dependence of the effective doping concentration N_{eff} and full depletion voltage as a function of 1 MeV neutron fluence.*

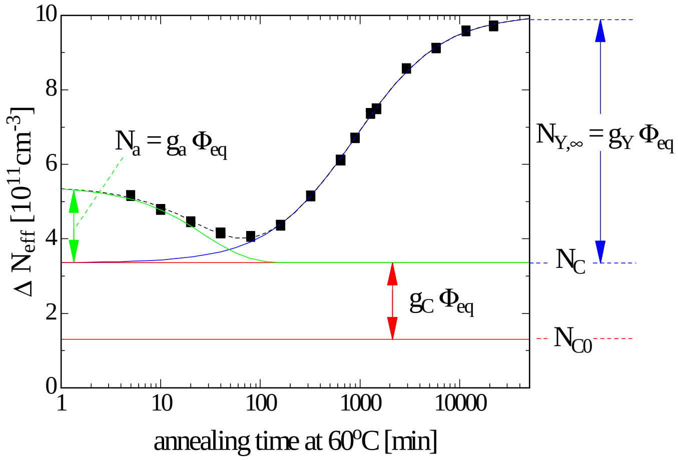


Figure 3.18: *Annealing curve showing dependence of ΔN_{eff} as a function of annealing time at $60°C$.*

CHAPTER 4

MODULE READOUT AND COMMUNICATION

"But what... is it good for?"

Engineer at the Advanced Computing Systems
Division of IBM, 1968, commenting on the microchip.

Contents

In this chapter the electronics used to communicate data to and from the modules are discussed. An overview of the steering and monitoring software associated with the electronics is given. The steps needed to optimise communication and calibrate the detectors are discussed. The front-end electronics are on the modules and thus in the active volume close to the interaction point. This necessitates that the electronics are highly radiation tolerant. This requirement has been implemented using special fabrication processes. The power supplies and a dedicated VME based readout system are located underground but at several tens of metres away from the detectors. This area is accessible during operation.

4.1 Signal Processing at the Front-end

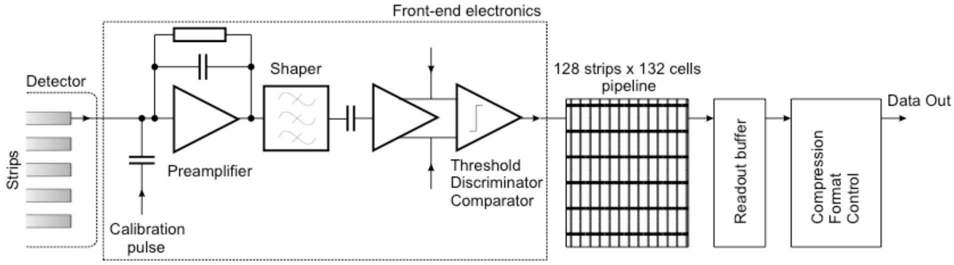


Figure 4.1: The basic readout chain at the front-end.

A particle traversing the detector induces a current in a strip. Figure 4.1 shows the basic stages of the readout process. The generated current signal is integrated in a charge sensitive pre-amplifier. At the output of this amplifier there is a voltage signal with an amplitude proportional to the total charge generated in the silicon strip. The characteristic time constant is $\tau_f = C_f \cdot R_f$, where C_f is the feedback capacitance of the charge sensitive amplifier and R_f is the effective resistance of the pre-amplifier:

$$V_{out}(t) = -\frac{1}{C_f}\int_0^t I_{in}(t)\,dt = -\frac{Q_{in}}{C_f}\,exp(-\frac{t}{\tau_f}) \tag{4.1}$$

The feedback resistor is put in parallel to the feedback capacitor in order to discharge C_f after each integration. The readout electronics collects the charge Q_{in} from its readout electrodes generated in the SCT detector in about 10 ns at the pre-amplifier stage.

In the next stage, the voltage signal is fed into the main amplifier known as a shaper. It provides the pulse shaping according to the timing requirements and it filters the noise in order to maximise the signal to noise ratio. The shaping time τ_s, is significantly higher than the charge collection time to avoid any charge losses due to the ballistic deficit (the loss in signal pulse height due to noise). The peaking time is 20 ns at the shaper stage, however it is closer to 25 ns once the charge collection is taken into consideration [18]. The signal is amplified by an amount defined by the shaper current. The SCT default setting is 30 μA, giving a gain of 50 mV/fC of charge at the input to the discriminator [18]. The discriminator is designed as a differential comparator. It detects the presence of a signal when the amplitude is above a pre-defined threshold. This threshold is controlled by a differential voltage applied to one of its input pins. When the signal is above this threshold, a “1” is registered and when it is below a “0” is returned. In this way, hit or no hit information is provided and is stored for each of the 128 channels of the chip. This binary readout allows the electronics to be simplified, since the data is reduced to only one single bit of information. This leads to a smaller chip which consumes less power than for a fully analogue system.

4.1.1 ABCD3TA Chip

One module is read out using twelve front-end ASICs, called ABCD3TA [29], which are fabricated using the radiation tolerant DMILL [31] process. During the SCT’s ten years

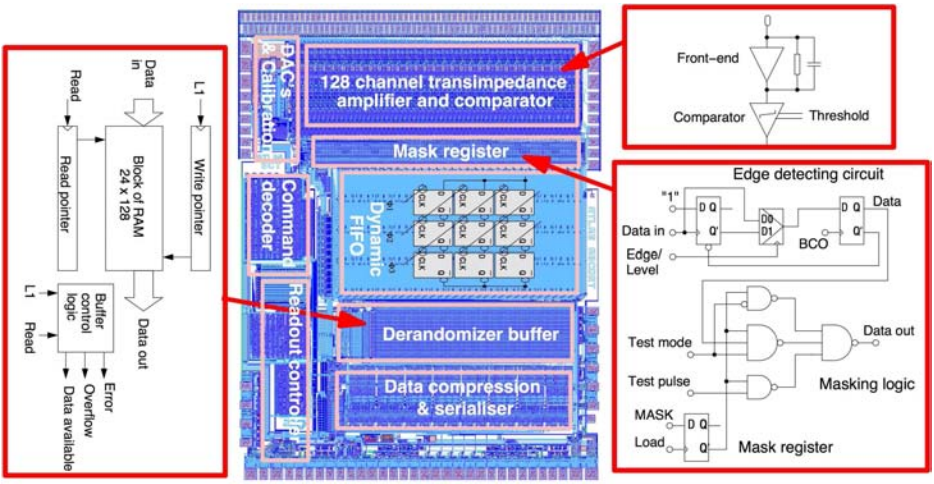


Figure 4.2: Block diagram of the ABCD3TA chip.

of operation at the design luminosity, a total ionizing dose of 10 Mrad and a fluence of 2×10^{14} 1 MeV neutron equivalent per cm^2 is to be expected. The chip design is strongly dependent on the required bunch crossing frequency of 40 MHz and the required radiation hardness. The binary design includes a four mode data compression circuitry, leading to a huge reduction in data being readout. This allows a more simplified off-detector readout-electronics as well as reducing the costs and amount of material needed for the transmission of data.

4.1.1.1 ASIC requirements

To arrive at a detector efficiency above 99 $\%$ for each module, the signals read out from each strip must reach above a threshold of 1 fC. The average signal is around 25,000 e for a MIP. The noise occupancy is also required to be below 5×10^{-4}. The data readout should have less than 1% data loss (resulting from chip overflows) at an average trigger rate of 100 kHz. The following list gives the basic functions that each chip requires in order to allow full testability throughout the various stages of testing, from production right through to running the experiment [29]:

- charge integration;
- pulse shaping;
- amplitude discrimination;
- data latching;
- data storage for Level 1 Trigger;
- data derandomisation and compression;
- data transmission.

In addition to this, a chip bypassing feature is added to allow the data to be continuously read out, even in the event of a chip failure.

4.1.2 Design Overview

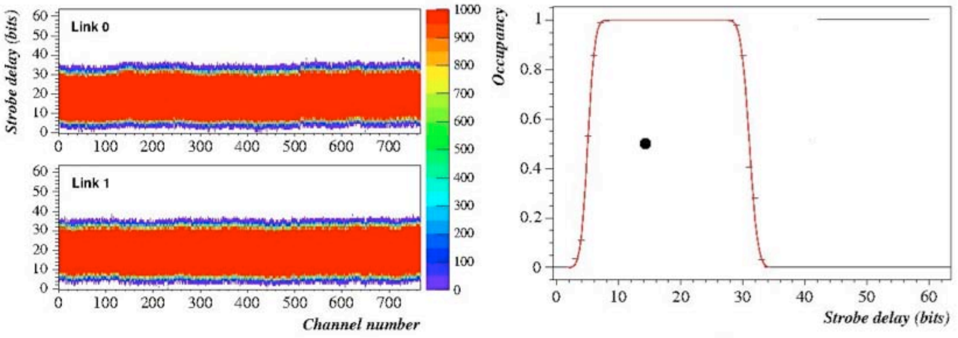
Figure 4.2 shows the basic functions which have been integrated into one single chip. It contains everything needed for a binary system: front-end circuitry, discriminators, binary pipeline, de-randomizing buffer, data compression logic and readout control logic. The front-end uses mostly bi-polar technology (≈30,000 devices) while the digital part uses approximately 200,000 CMOS devices. In the next sections we will discuss fully the internal calibration circuitry, followed by a short description of each building block of the chip design.

4.1.3 Front End Internal Calibration

To determine the gain for each individual channel, a controlled signal is induced into the amplifier. The Digital-to-Analogue-Converter (DAC) sets the height of the calibration pulse. A voltage step is generated through an internal calibration capacitor (of 100 fF) connected to it's input, in order to simulate a hit strip. There are four calibration lines, providing a signal to 32 channels simultaneously on each chip, allowing testing of groups of channels.

The timing of the injected signal is crucial for the accuracy of the gain measurement. The pipeline looks at the output from the comparator at the rising edge from every clock cycle. To adjust the "*sample*" time a strobe delay scan is performed. This scan varies the delay between the calibration pulse and the clock pulse, and the occupancy is recorded. (Meaning the number of times the signal is greater than the set threshold). For each value of the strobe delay, a fixed number of triggers (usually 1000) is sent to each chip. The occurrence of a "1" and "0" is counted. Similar scans are made for determination of optical threshold. Figure 4.3 shows the raw occupancy and strobe delay plots for a scan using the data acquisition software. The number of hits is indicated by the colour. The 40% of the active window is taken to be the ideal delay setting. The threshold of the comparator can be controlled to optimise between noise occupancy and efficiency , so that a choice can be made on what qualifies as a registered hit. By varying this threshold whilst injecting a calibration signal of a fixed size, an S-curve (so-called because of its shape) is produced. It is the number of hits as a function of threshold. In an ideal situation where no noise is present, a continuous hit pattern would be registered until a point where the threshold is above the signal height. In this situation the noise occupancy would drop to zero. For the signal distribution of real particles the S-curves follow the integral of a Landau distribution. In reality, however, this is not the case, since noise distorts the shape of the signal and can either add or subtract to the overall pulse height, giving rise to fake hits. The smearing of the threshold curve is due to the noise on the signal. The steepness of this S-curve is a good indication of the amplitude of the noise. Figure 4.4 shows a single channel plot for an injected input charge of 3 fC. On the left is a histogram of the hit occupancy as a function of the threshold for 1000 events. On the right is the noise distribution which has a Gaussian amplitude distribution. The S-curve for a fixed charge and Gaussian noise is described by a complementary error function. The threshold which gives an occupancy of 50% , is the threshold corresponding to that input charge. It is known as the VT_{50} point. By fitting the S-curve to this error function defined as:

$$erf(z) = \frac{2}{\sqrt{\pi}} \int_{z}^{\infty} e^{-x^2}\, dx \qquad z = \frac{\mid V_{thr} - \mu \mid}{\sigma}, \tag{4.2}$$



(a) (b)

Figure 4.3: On the left (a) typical raw data plots for both sides of a module. Colour represents the hit occupancy and white represents zero hits. On the right (b) the profile of the occupancy for one chip, fitted with a product of an error function and complementary error function, giving a smoothed top-hat shape. The black dot represents the ideal strobe delay value, set 40% along the active window of the x-axis.

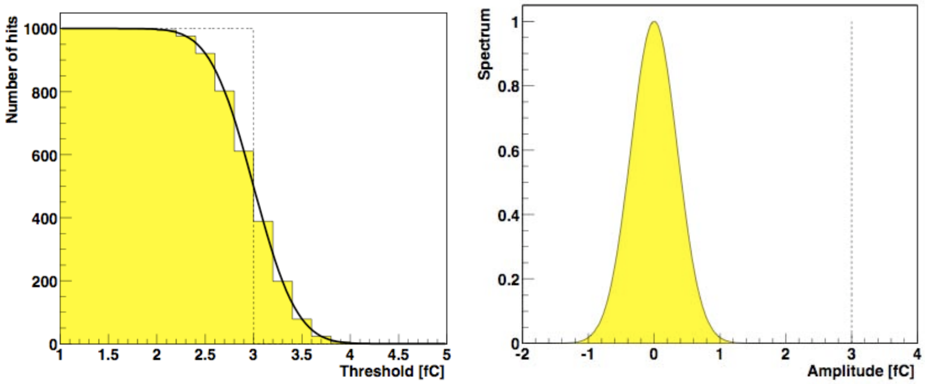


Figure 4.4: This histogram gives the number of times the signal was greater than the threshold. On the left, the threshold is increased in 0.2 fC steps and the signal readout 1000 times.The dashed line shows what would be the ideal readout of the system, in the absence of noise. On the right is a plot of the Gaussian distribution of the noise.

the noise and the median can be extracted. The derivative of this error function gives the noise distribution:

$$P_G(V_{thr}, \mu, \sigma) = \frac{1}{\sigma\sqrt{2\pi}}\, e^{-\frac{1}{2}\left(\frac{V_{thr}-\mu}{\sigma}\right)^2}, \tag{4.3}$$

where V_{thr} is the threshold voltage, μ is the median of the detector signal (the 50% point of the threshold scan) and σ is the RMS noise of the detector. The measured σ is the noise taken after the signal amplification process. Therefore, this noise is a measurement of the output of the analogue part of the ABCD chip. Each point on the S-curve can be fitted using equation 4.3 to give a value for the input noise (fC) at a particular threshold. This is shown on the right-hand plot of Figure 4.4. The important quantity is the noise at the input to the amplifier. To calculate the input noise, the gain of the amplifier must be determined. The small signal gain is the ratio of the output voltage of the amplifier compared to the difference in input charge injected at the input to the amplifier. It is expressed in mV/fC[1].

$$\text{small signal gain} = \frac{6250 \times \text{output voltage}}{\Delta\text{input charge}} \quad \left(\frac{\text{mV}}{\text{fC}}\right) \tag{4.4}$$

Threshold scans are taken for several input charges. Their median values, μ, also known as the response, are plotted versus input charges. A *'Three Point Gain'* scan injects three charges of 1.5, 2.0 and 2.5 fC during a threshold scan. A linear fit is applied to the three VT_{50} points using:

$$y = ax + b,$$

where y is the VT_{50} point (from complementary error function fit) in mV, x is the injected charge in fC and the parameters to be determined from the fit are *a* (the approximation of gain in mV/fC) and *b* (the offset in mV). When 10 charges are injected, ranging from 0.5 fC up to 8 fC, this is called a response curve (see Figure 4.5). The VT_{50} points of each S-curve are this time fit to a linear function with an exponential correction term given by:

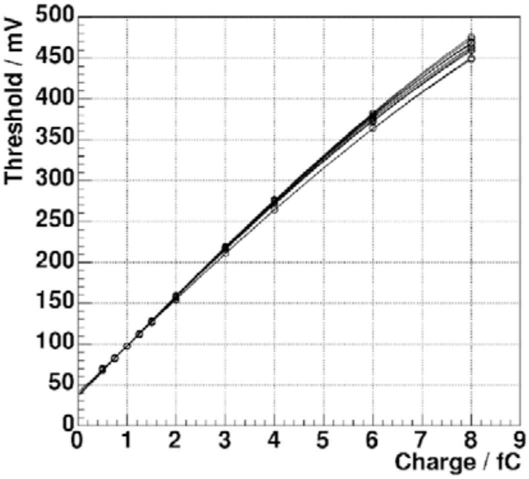


Figure 4.5: The response curve showing the VT_{50} points of several injected charges for one module with 12 chips.

$$y = p_2 + \frac{p_0}{1 + e^{-\frac{x}{p_1}}} \tag{4.5}$$

The gain, is taken to be the slope of the fit, determined by

$$\text{gain} = \frac{dy}{dx} = \frac{p_0 \cdot (e^{-\frac{x}{p_1}})}{p_1(1 + e^{\frac{-x}{p_1}})^2} \tag{4.6}$$

where the three fit parameters p_0, p_1, p_2 are: the measure of non-linearity, the small signal gain and the offset (average output when no charge is injected). A nominal front-end gain is approximately 50 mV/fC, corresponding to a signal input range of 0 - 12.8 fC. The input noise is computed in the same way as given by equation 4.4.

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[1] 1fC is equivalent to $\approx 6250e^-$.

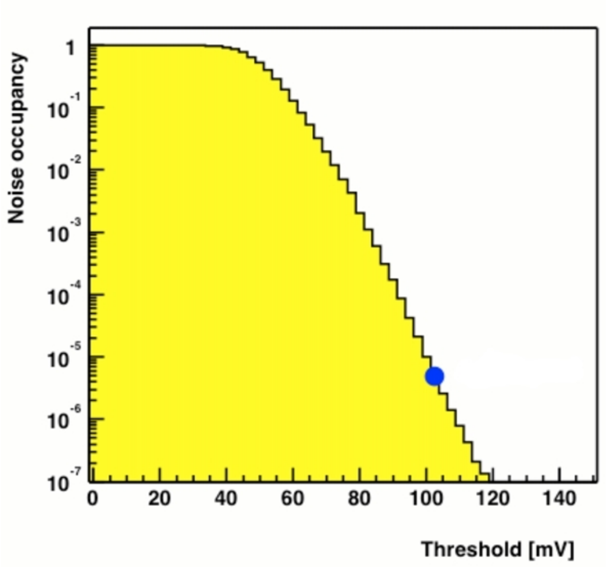

Figure 4.6: Noise occupancy versus threshold (mV) for no charge injection. The final noise occupancy value is taken to be the occupancy at the operational threshold of 1 fC, denoted by the blue dot.

The noise occupancy is defined as the percentage of random hits that are noise induced. No signal is injected and the occupancy is calculated for the 1 fC threshold point. A threshold scan varying from 0 - 1.5 fC is performed. With a higher threshold comes a lower number of hits, therefore the number of triggers is increased. The maximum number of triggers is 1 million. The scan stops when only a few hits are registered in the module. By plotting the log of the occupancy vs threshold^2, and then fitting a linear function, an estimate of the noise can be calculated. This can be compared to the input noise measured by either the 3Pt Gain or Response curve tests. Using both independent methods, a cross check of the set-up is achieved.

The threshold of 1.0 fC is the nominal operational value of modules in ATLAS. Therefore, the requirements are for an occupancy of $< 5 \times 10^{-4}$ at this given point. Figure 4.6 shows the threshold versus occupancy plot for a typical module. The value denoted by the dot is the noise occupancy at the 1 fC point.

The threshold voltage of the discriminators is common for all channels, and is generated by an internal 8-bit DAC, programmed via the control logic. It is tunable from 0 - 640 mV with a step-size of 2.5 mV. The critical factor in a binary scheme is the spread of the DC level from channel to channel at the discriminator inputs. The sources of this spread are the offsets at the input stages. The differences at the inputs are affected by the front-end circuitry gain for that particular channel. To compensate for this, a threshold correction for each channel exists using a 4-bit trimming, named TrimDAC. Two additional bits set the range of the TrimDAC step. Step sizes of 4, 8, 12, 16 mV correspond to a total range from 0 - 240 mV, with a threshold spread = step(mV)/$\sqrt{12}$. In case a channel is defective or noisy, a mask register can be used to switch off a particular channel. This reduces the number of fake hits in the data, as well as providing useful test patterns to the pipeline during chip testing.

Pipeline

The pipeline stores the data for up to 132 bunch crossings. On each clock cycle a pointer is moved from one column to the following one and the hits are stored. Once the LVL1 trigger is received, the corresponding data column is marked for readout, in addition to the data from the previous and next bunch crossings. This is referred to as the "*three time bins*" readout. The derandomising buffer is a second level buffer, 24 bits deep, allowing 8 events (8×3 time bins) to be stored in memory for each of the 128 channels. Its purpose is to accommodate rate fluctuations from the LVL1 trigger distribution. In order to reduce the number of bits to be read out, the data compression logic has four selection modes. Table 4.1 gives the allowed logic modes.

Each three bits of data is compared to the required hit pattern according to the selection criteria. If there is a match then the three bits get sent to the readout circuits for transmission. If there is no match then the next channel is compared to the selection criteria. The channel numbers at the beginning of the hit cluster followed by the hit patterns within the cluster are sent to be read out.

selection criteria	hit pattern	usage
hit	1XX, X1X, XX1	detector alignment
level	X1X	normal data taking
edge	01X	normal data taking
test	XXX	test mode

Table 4.1: The four selection modes in the compression logic. At each event the three time bins are read-out. "1" indicates a hit, "0" indicates no hit and X can be either state.

Data Readout and Redundancy

The newly suppressed data is read out via a token ring for the six chips on each side of the module. The chips can be configured in three different modes, *master*, *slave* and *end*. On link 0 of the module, the first chip is known as the "master" M0, followed by four "slaves", S1, S2, S3, S4 and finally an "end" E5. The master is connected to the optical links driver for data transmission. Similarly on link 1 there are the following chips: M8, S9, S10, S11, S12, E13. Each chip has a pair of token and data input/output lines. When the LVL1 trigger is received, the readout begins with the Master chip. It sends the pre-amble bits at the beginning of each data read out. This consists of a bunch crossing and level 1 identifier. Next, the master sends its own data to the optical readout driver before sending the token to the next chip on its right. This slave then responds to this by sending its data to the master, which in turn appends it to the readout circuitry. Now the token is passed to the next chip in the chain. Its data is sent back to the master via the other chip in the chain. This process is repeated until the last chip is reached. It sends its data along with a trailer which tells the master that it is the "end" in the configuration and that the data stream is finished. Once the master sees the trailer it knows that all the data from the event has been sent. It now begins the data transmission for the next event.

Should one chip fail, a redundancy scheme exists. This allows the data and tokens from the remaining chips to be routed around the failed chip. If an end chip fails, then the previous slave is programmed to readout as an end. In the case where a master chip fails, the data and tokens can be routed to be read out via the other master on the opposite link.

4.1.4 Single Event Upsets

High energy particles passing through the detector also deposit energy inside the front-end chips. This local free charge creation can create malfunctions in the front-end electronics. If data in a memory chip becomes corrupted, but the chip remains undamaged, this is known as a soft error: a single event upset. A bit flip in the pipeline causes a single data error and it does not require any intervention. However, errors in the static register may lead to changes in the operating mode of the chips and will require a re-loading of the chip configuration. The single event upset is not destructive to the circuit functionality, unlike the case if a single event latch-up. A latch-up is the inadvertent creation of a low-impedance path between the power supply rails of an electronic component. This triggers a parasitic structure, which then acts as a short circuit, disrupting proper functioning of the part and possibly even leading to its destruction due to over-current [33]. The manufacturer's design of the ABCD3T chips, has ensured that latch-up does not occur as a result of the striking particles.

4.2 Optical Communication and Readout

Optical links are used to transfer the data from the modules off-detector, as well as to distribute the bunch crossing clock, level 1 triggers and commands to the modules. The next sections will give an overview of both the on and off detector components as well as the interfaces necessary for the complete readout and control of the SCT.

4.2.1 Optical links Architecture

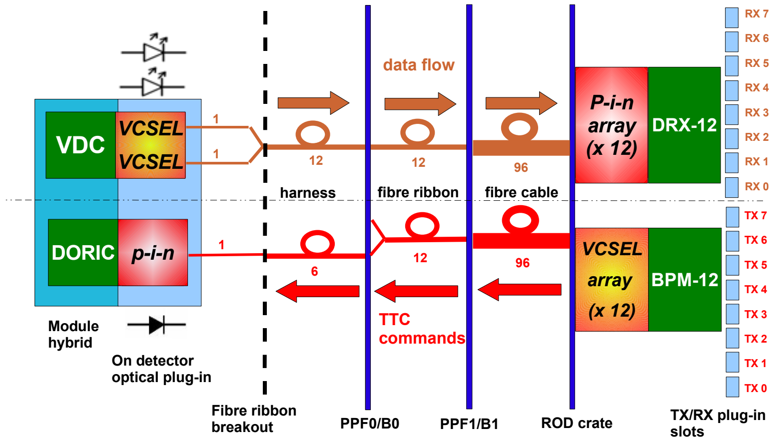

Figure 4.7: An overview of the SCT optical link architecture.

The optical links are based on using Vertical Cavity Surface Emitting Lasers (*VCSELs*) for transmission of light signals, and epitaxial Si *p-i-n* diodes for the receiving of light signals. For each module, two data links and one Timing, Trigger and Control (TTC) link exist. The data links are operated at 40 Mbit/s, transferring data from the modules off the detector. The links which send the TTC commands are called TX links since they *transmit* signals, and the data links are called RX links due to the fact that they send the *received* data back from the module. The *VCSEL*s emit light at 850 nm and were chosen due to their high robustness to radiation damage, as well as their extreme, bright light source and low power consumption. Figure 4.7 gives an overview of the architecture of the optical links.

TTC and Data Links

The back of crate card (BOC) in the counting room provides the interface between the optical signals and the off-detector readout electronics. The TTC signals are sent to each module with the use of a BPM-12 (Bi-Phase Mark encoding) ASIC. It combines the 40 MHz bunch crossing clock and the 40 Mbit/s command into one single data stream (see Figure 4.8). Each ASIC drives an array of 12 *VCSEL*s, allowing up to 12 modules to be read out. The data is sent optically via a radiation hard optical SIMM (step index multi-mode) fibre. The optical signal arrives at the modules and is converted into an electrical signal by a *p-i-n* diode. Its electrical output is fed to the DORIC4A ASIC which transforms the signal into the original individual clock and control data streams. Each BPM-ASIC has a built in course and fine delay adjustment. This ensures that the LVL1 trigger arrives at the ABCD chips at precisely the right time. There is also a built in redundancy for the TTC links, should a module fail to receive its commands. Electrical connections exist between each module which allows a copy of the neighbouring TTC commands to be sent to the failing TTC link module.

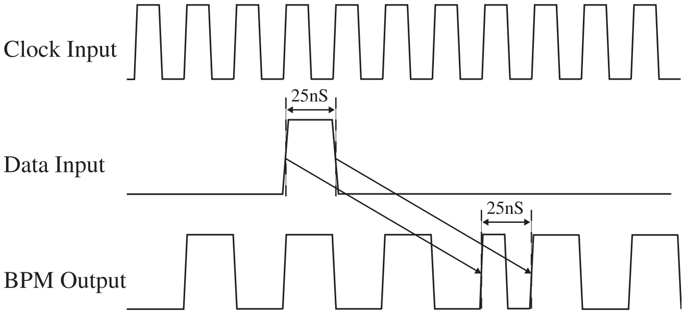

Figure 4.8: The Bi-Phase Mark encoding scheme. The top signal contains the bunch crossing 40 MHz clock and the middle signal gives the 40 Mbit/s control signal. The two signals are combined to give the bottom signal in the figure.

The master chips on each module side, sends all of the data from their 6 chips to the *VCSEL* Driver Chip (VDC). Here the VDC drives two *VCSEL* channels and the signal is converted from electrical into optical for transmission to the off detector electronics. The data is sent in an NRZ format (Non Return to Zero) at a transfer rate of 40 Mbit/s. The *VCSEL* can be controlled from its current, which is determined by its voltage. Only one voltage controls both *VCSELS*, setting the current between 0 -20 mA. By default they are both set to 10 mA during operation. The *p-i-n* arrays at the BOC convert the optical signal into an electrical stream which is received by the DRX-12 ASIC and translated by the Read-Out Driver (ROD). The DRX ASIC is used to amplify and discriminate the electrical signals output from the *p-i-n* diodes. Each channel on the ASIC has an adjustable threshold which can be set using an external reference voltage, to set a threshold ranging from 0 - 255 μA. This threshold is set individually for each channel in order to reproduce the data signals from the modules.

Opto-package and Optical harness

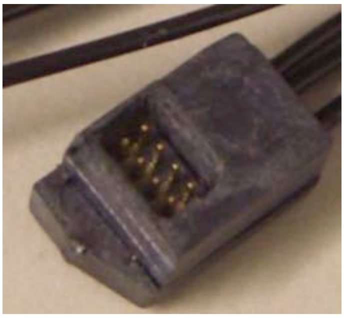

Figure 4.9: Close-up of the opto-plugin connector

The opto-package consists of mounting and bonding the *VCSEL* and *p-i-n* diodes onto a PCB board. The optical fibres at each connection are actively aligned to give an optimal coupling for the transmission and reception of light signals. Custom parts made from black infrared, strongly absorbing material, ensure that no electrical/optical cross-talk between the *VCSEL*s and *p-i-n*s will occur. The fibres are also encased in a 900 μm diameter black furcation tubing, so that no significant light leakage can occur which would result in a higher noise detected in the silicon sensors.

The barrel opto-packages are located on the detector but not directly on the modules themselves. They are mounted onto a separate copper/kapton flex circuit. One end connects directly to the modules, the other to a PCB which connects to the power tapes. The opto-package for the endcaps is located on the module via an electrical connector.

SIMM fibres transport the optical signals to and from the modules. The pure silica core ensures radiation hardness. The optical harnesses are designed to read-out up to 6 modules. In the case of the barrel, a total of 352 harnesses were needed. They differ from the endcap harnesses since they combine the low mass power tapes with the optical harness into one entire unit. For the endcap, seven different harness types read out between 4 and 6 modules. The data ribbons and TTC ribbons are separated from each other and fusion spliced to a 12-way SIMM fibre. Since only up to 6 fibres are needed to send the TTC commands to the modules, only the central most fibres are used. The fibres are wrapped in aluminium foil due to the close proximity of the modules. This prevents any unwanted leakages of light.

In order to reduce the number of unused fibres within a 12-way SIMM fibre, it is split into two 6-way ribbons called a Y-ribbon. Each end is terminated with a MT-12 connector allowing a connection to two 12-way fibres, delivering commands for up to 12 modules.

4.2.2 Module Communication Optimisation

To allow for a stable data communication between the modules and the readout acquisition, the optical settings for the readout must be optimised. Various tests are carried out to ensure the best working set-up with regards to sending data to the modules as well as reading back the data. The timing and control signals are sent from the off-detector *VCSEL* arrays to the DORIC chip on the module front-end for decoding (see Figure 4.7). The intensity of light that carries the signals has to be set correctly, to avoid any errors in the data stream. A test is performed to find the best setting for which there are no errors and whereby the DORIC is not saturated. By carefully monitoring the current induced on the receiving on-detector *p-i-n* diodes, the correct value can be determined.

The DORIC on the detector which decodes the control and command electrical signals from the on-detector *p-i-n*s, requires that the duty cycle of the bi-phase encoded optical signal is set to 50%. This is to ensure that the original clock pulses are decoded effectively without any jitter. A test exists to optimise these settings.

The next stage in the optical settings is optimisation of the receiving light which contains the data from the modules. The *VCSELS* on the optical plug-in send light to the off-detector *p-i-n* diodes. The time delay of the optical receiver relative to the data signal must be tuned. Next, the discriminator threshold needs to be set for the off-detector decoding ASIC (DRX-12 in Figure 4.7) to distinguish between hit (1) or no hit (0) data. A data packet is sent to the decoding ASIC and the threshold varied to find the working region in which no errors were returned. The minimum and maximum threshold settings are determined, and the best value taken to be the 75% point of the difference between the two values. Figure 4.10 shows the output data from a scan using the data acquisition software.

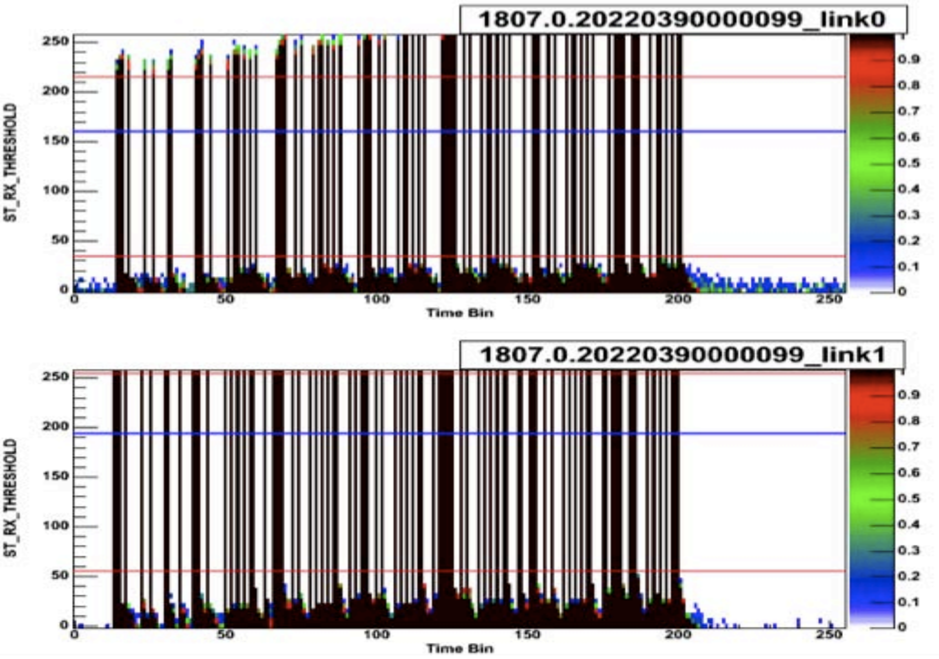

Figure 4.10: The raw data output from an RX threshold scan. Here both links are returning the required data packets and the receiving threshold is varied. The red lines denote the minimum and maximum RX threshold values and the blue line is the most optimal RX setting for the receiving of data.

On the x-axis is the time and on the y-axis, the varied receiver threshold. There are two plots, one for each link reading the data from the module side. The black points indicate that a hit is being returned. There is a dot for each value of time and threshold. (If the hits are found at any threshold this will result in a vertical line.) The structure of the pattern is similar since the data packets are sent in a defined time sequence. In the upper plot, between the time bins of 0 and 50, the errors are detected by the colour points at the top. The maximum threshold is set just below the errors. On the lower region of each plot, there is a low black background which is present. This is caused as a result of the slow turn-off of the *p-i-n*s receiving the light off-detector. The minimum threshold is therefore set just above this background. The middle line represents the optimal discriminator threshold for the link.

An overview of the tests which optimise the optical settings, as well as those which test the digital and analogue functionality of the module chips are described in appendix B. Having described the front-end electronics and the optical architecture, the following section will concentrate on the software that is in place for controlling and monitoring the SCT detector.

4.3 Detector Control and Monitoring

To ensure the safety and to check the quality and performance of the detector, various parameters are constantly being monitored. Whenever the temperature of a module becomes too high, it is switched off. In case of malfunction in a part of the cooling circuit the power to the module is disabled. The stability of the LV is important since it results in a good performance of the read-out ASICs as well as the optical links reading the data to and from the detector. The stability of the LV and HV reduces the amount of noise to the system as well. The constant monitoring of the temperature and humidity of the SCT support frame are important to be aware of serious changes that could alter the shape of the detector structure. We will begin with a short introduction to the hardware architecture explaining each of the parameters monitored, followed by an overview of the two main software projects: DCS and SctRodDaq.

4.3.1 Power Supply and Environment Projects

The detector control system (DCS) serves to monitor and control the power supply and environmental aspects of the detector, ensuring a safe functionality. Here, a short overview is presented, but for more detailed reading, see references [20] and [4]. The system can be simplified by discussing the main parameter categories; low voltage, high voltage, cooling and temperature monitoring.

1. Low and High Voltage

In total, there are 88 power supply crates distributed between the two counting rooms USA-15 and US-15 in the ATLAS cavern. The power supply system uses a modular structure with each crate containing twelve LV cards with four output channels and six HV cards with eight output channels. Each crate is capable of powering up to 48 modules. For grounding and shielding purposes, the two power supplies are floating independently, with all voltages being grounded on the outer thermal enclosure described later in section 5.1.5. The LV supplies provide the analogue and digital power to the front-end ASICs as well as to the DORIC and VDC chips needed for the optical readout (see Figure 4.11). The *p-i-n* and *VCSEL*s located on the optical links connected at the module hybrid, also receive their voltages from the LV supplies. Due to the long power cables between the modules and the power supplies ($\approx$ 90 m), typical voltage drops across the cables are between 0.5 and 0.8 V. Four sense-wires allow the exact control and setting of the analogue and digital voltages Vcc and Vdd respectively.

Lastly, the HV cards supply the bias voltage to the modules, which controls the active depletion area of the module. A module can be biased up to 480 V after irradiation for the depletion of the sensors. A firmware protection schemes exists for both the HV and LV supply channels. In the case that the limits of a parameter are exceeded, the hardware logic sends a signal to the corresponding HV or LV channel which will in turn cause it to trip. Table 4.2 gives the limits for the 14 (13 for the endcaps) parameters associated to each module.

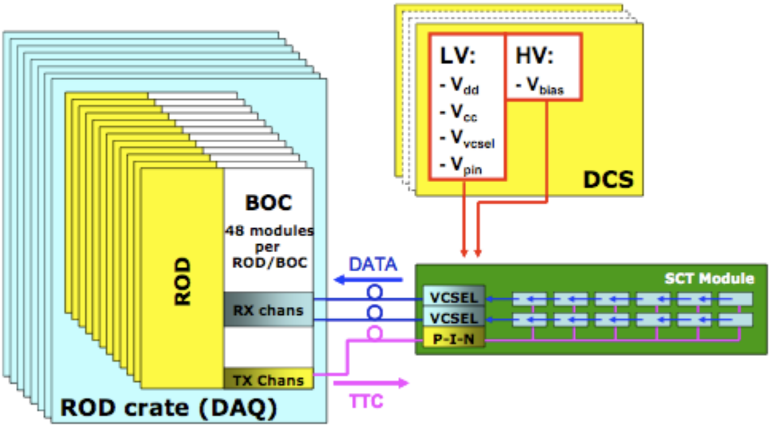

Figure 4.11: Schematic showing the module powering and communication scheme.

Table 4.2: The 14 parameters associated to each barrel module on the detector (13 for the endcaps), indicating their typical and maximum values, hardware trips and limits, programmable firmware trips and crate controller trips.

	Parameter.	Typical	Max	HW Trip/Limit	FW trip	CC trip
VOLTAGE	Vbias	150 V	480 V	480 V		10 V
	Vcc	3.5 ± 0.2 V	5.1 V	5.1 V	10 V [a]	
	Vdd	4.0 ± 0.2 V	5.1 V	5.1 V		
	VccPS	5.1 V [b]	10 V	10.2 V		
	VddPS	5.0 V [b]	10 V	10.2 V		
	VVCSL	4.0 V	6.6 V	9.6 V [c]		
	VPIN	6.0 V	10 V	13.0 V [c]		
CURRENT	Ibias	0.3 μA	5 mA	5 mA	5 μA	3 μA
	Icc	900 mA	1300 mA	1500 mA		
	Idd	580 mA	1300 mA	1500 mA		
	IVCSL	2 mA	10 mA	10 mA [d]		
	IPIN	0.2 mA	2 mA	2 mA [d]		
TEMP	T1	0°C	29-56°C		> 38°C	
	T2	0°C	29-56°C		> 38°C	

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[a] Only applicable for channel in OFF state.

[b] Typical voltage drops in return lines are 0.8 V for Vcc and 0.5 V for Vdd.

[c] A maximum voltage drop of 3 V in digital return line is included.

[d] Current limits and do not result in a trip.

2. Cooling and Temperature monitoring

There are temperature and humidity sensors placed at different location throughout the detector, mapping its environmental conditions. This includes the temperature sensors located on the modules themselves as well as the carbon fibre support structure. The temperature and humidity of the air within the detector volume is also closely monitored. Radiation hard humidity sensors register the dew point of the volume, indicating when the system is safe enough to be cooled without any risk of condensation to the modules. Temperature sensors are also placed on the cooling pipes of the structure and at their exhausts. These sensors are linked directly to a hardware interlock system, giving high protection to the modules in the event of a cooling failure.

To monitor the temperature of the module, there is a Negative Thermal Coefficient resistor (NTC) mounted directly on the module hybrid (2 for the barrel, 1 for the endcap). The current necessary for their read-out is distributed by the LV cards.

3. Safety

To stop the system in the event of serious cooling failures, a hardware interlock exists to ensure the absolute safety of the SCT subsystem. There are many cooling loops throughout the detector. Each connects 48 modules (or up to 33 in the case of the endcaps). On each loop there are two temperature sensors, that verify to the interlock system that the temperature of the pipes are cold enough before powering the modules.

Responsible precautions are also necessary for the optical read-out system which is used. To allow the safe operation of the *VCSEL* arrays housed in the BOC, an interlock is in place. If the door to the DAQ unit, containing the BOC *VCSEL* arrays is opened, then the power to the *VCSELS* is immediately cut-off.

4.3.2 Data Acquisition System

Here an overview is given of the off-detector read-out hardware that is in place, providing an interface between the on-detector front-end electronics and the data acquisition system. Several components make up the structure of the DAQ hardware system which allows the control, monitoring and configuration of the modules. A VME crate stores the components given in Figure 4.12. In total there are 8 crates, each one containing up to sixteen Read-Out Drivers (RODs), sixteen Back Of Crates (BOCs), one Timing Interface Module (TIMs) and one ROD Control Crate (RCC). The front of the crate holds the ROD/BOC pairs, and

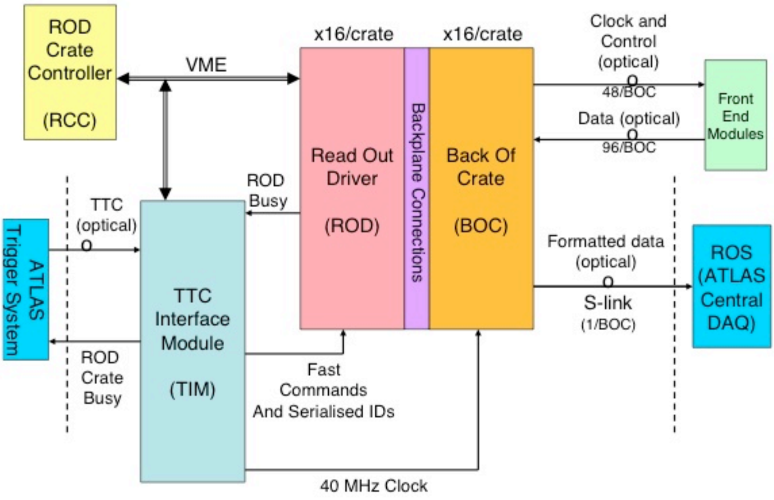


Figure 4.12: A schematic of the DAQ hardware architecture.

connecting the RODs to the BOCs is a custom made back-plane enabling the communication between the two. The TIM is placed in the middle of the crate which allows for the transfer of ATLAS TTC signals to the ROD/BOC pair. The RCC is a single board computer (SBC) which is situated in the first slot of the VME crate. It is the crate master providing configuration and control of the components within its crate.

1. TIM

One TIM is capable of sending information to a maximum of 768 modules. The TIM interfaces the TTC signals from the ATLAS first level trigger to modules. Once the LVL1 trigger information is received by the TIM, it decodes the relevant data before passing on the information to the different sub-components. In the event of a failure in the receiving of the clock from the LVL1, the TIM generates its own replacement local clock. The BOC allows a delay in the output timing of the TX plugin signals, which send the clocks to the modules sent by the TIM. There are two types of timing to consider: global and local. Global timing corresponds to the timing of the SCT as a whole relative to the time of the event's primary interaction. The local timing is the synchronisation of all the modules in relation to one another. The local synchronisation ensures that the clock sent to the module front-end has the correct phase relative to the time of flight (TOF) of particles from a collision within the detector. This is due to the different optical fibre lengths associated to each module location, and hence this phase must be set individually for each module. It is also essential to the front-end read-out that the TTC signals from the LVL1 trigger received by the TIM are timed in properly to ensure the readout of the correct event to maintain a synchronised Bunch Crossing ID (BCID).

2. ROD

The ROD is responsible for the data of up to 48 modules. Its job includes configuring the modules, sending triggers, formatting event data, calibrating the detector modules as well as providing monitoring. It can operate in two modes. In calibration mode it is able to generate its own internal triggers without the need for the TIM module. In physics data taking mode it is able to format the module hit data received and decoded by the BOCs before sending this data to the Read-Out Subsystem (ROS which is the ATLAS central DAQ) via optical S-Links. In both modes it is also capable of histogramming the raw data from an event. The RODs in the readout crate, receive the trigger and command signals and then distribute them to the modules. The clock signal is sent to the associated BOCs.

3. BOC

Paired with each ROD is a BOC. It sends the commands given by the ROD to the module front-end. The BPM-12 and DRX-12 chips, mentioned in section 4.2.1 are housed within the BOC as well as the *p-i-n* and *VCSEL* arrays, named TX and RX plug-ins. So called because TX stands for Transmitter and RX for Receiver. There are 4-TX plug-ins (0-3) and 8 RX-plug-ins (0-7) (one for each side of the module). The 40 MHz clock is received by the TIM and distributed via the BPM-12 chips and *VCSEL* arrays to the modules. The *p-i-n* arrays receive the data which is then discriminated by the DRX-12 chips and formatted by the RODs, before being passed back to the BOC, ready for sending to the Read-Out-Subsystem via optical S-Links. There is only one S-Link for each BOC, containing the event data for all possible 48 modules.

4.3.3 Data Acquisition software

The data acquisition software, SctRodDaq [66],[14],[15], provides an interface between the hardware, previously described, and the front-end modules. It does so by communicating directly with the VME masters of the ROD crates. It allows for the control and monitoring of various configurable module settings, as well as providing an interactive mode for calibrating and displaying the corresponding results. A Java-based graphical user interface (GUI) exists which allows the user to interact easily with the modules on the detector. From here, the user can initiate a characteristic test sequence or individual calibration tests on the modules. Views of the barrels and discs enable the user to interactively "click" on a module to find out DCS information as well as being able to review the resulting test data. Modules can be individually selected to be in the configuration which dramatically helps to speed up the process of debugging problematic modules. By using colourful displays, an easy understanding of the module groups and test results is achieved.

The configuration of each detector module is achieved via an Extensive Mark-up Language (XML) file. For final ATLAS running, these files will be located in a CORAL database [38] ready to be uploaded by the DAQ and stored in the RODs. There are 9 servers in total in USA-15, of which 5 are dedicated to the barrel, and the remaining 4 for the endcaps. Many separate XML files are linked together to contain all the information necessary about the module configuration. As explained in section 4.2.1, the modules are all grouped together in opto-harnesses. Each group is called a Minimum Unit of Readout (MUR). The information in each MUR details the mapping and optical settings between the MUR and ROD/BOC pair. The modules on the barrel are all identical and as a result, the MUR structure is extremely modular. For the endcap, their configuration is more complex due to the different module types and positionings on each disc. Appendix A gives details on the configuration of the endcap modules, whilst reference [30] gives a good overview for the barrel.

CHAPTER 5

ENDCAP-A: DESIGN AND ASSEMBLY

"Be precise. A lack of precision is dangerous when the margin of error is small."

Donald Rumsfeld

Contents

5.1 Design of the Silicon Tracker Endcap

Nikhef was responsible for the complete assembly of endcap-A, one of the two endcaps that form part of the SCT. Various institutes from the UK participated in the assembly of the other endcap (C). This chapter aims to give an insight into each step of the assembly chain, explaining the extreme engineering accuracy that has resulted in a tracker endcap that meets the specifications. Endcap-A was transported to CERN in April 2006 where it underwent its final stages of completion. After the addition of the thermal enclosures and mechanical supports, it was integrated with the TRT. In May 2007, the endcap was installed in its final position in the ATLAS cavern. The following sections give a more detailed description of the endcap layout, which was first described in Section 2.5.3. It gives a clear description of the different components and interfaces needed in the design of the SCT detector endcap.

5.1.1 Support Structure

There are two single endcaps - A and C. The A-side is the name given to the section that is situated on the side of the positive Z-axis, and the C-side is for the detector located on the negative side of the Z-axis. For each endcap, 988 modules are mounted onto nine carbon-fibre support discs. The two skins of the discs are separated by a honeycomb core. The choice of materials ensures that deformations of the physical shape of the detector are minimal. Each carbon-fibre disc contains modules as well as their associated 'services'. These services include the power tapes giving the power to the modules, the optical fibres responsible for sending and receiving of data, the cooling pipes keeping the module temperatures low and many sensors with connecting cables to monitor the humidity and temperature of the structure. Completed discs are housed in a cylindrical support structure, with slots to hold each of the nine discs in position. There are also several apertures for the routing of the services. At each disc edge, the services are routed to (from) the disc surface, along the side of the supporting cylinder to (from) the end furthest from the interaction point. These services exit the SCT via a Services Thermal Feed Through (STFT), and run along cable trays to the end of the ID volume. In addition to the structure, there is also a front and rear-end support panel for each disc to sustain the weight of the SCT when it is mounted onto the TRT rails, allowing the SCT and TRT to share a common axis. Figure 5.1 shows the exploded view of each of the support components. The support cylinder is wrapped with a copper-polyimide sheet for grounding purposes.

5.1.2 Layout of Modules on Discs

An endcap contains nine discs (numbered 1-9), each populated with modules in such a way to ensure that the η coverage is optimised. There are three rings of modules, 52 outers, 40 middles and 40 inners. Discs 2-6 are identical and fully populated with modules. Discs 1,7 and 8 require only outers and middles and for disc 9, only a single ring of inners is required. Disc 8 needs only a short middle, since having a full middle module would not have any optimizing effects on the η coverage. Disc 9 was rotated to have the modules facing away from the interaction point to maximise the η coverage. The outer and inner modules are mounted onto the disc support on the side facing the interaction point. The middles are mounted on the opposite, lower z, side. In this way, the radial gap is filled where the front-end electronics and services from the outer and inner modules lie.

Table 5.1 gives a summary of the disc positions for the endcaps. One side of the endcap

Figure 5.1: An exploded view of the components which make up the support structure.

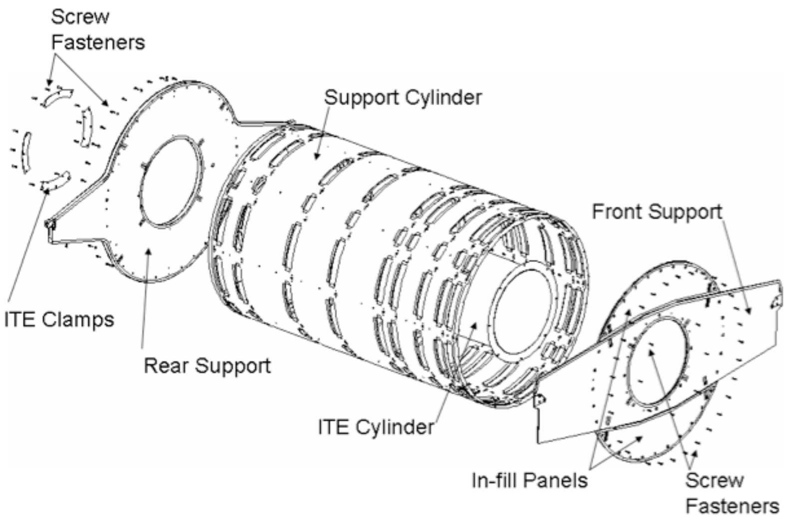


Table 5.1: The nominal z-position of the centre of each SCT endcap disc and the number of modules on each disc.

Disc	1	2	3	4	5	6	7	8	9	Total
$\|z\|$ (mm)	854	934	1092	1300	1400	1771	2115	2505	2720	
Outers	52	52	52	52	52	52	52	52	52	468
Middles	40	40	40	40	40	40	40	-	-	280
Short Mid	-	-	-	-	-	-	-	40	-	40
Inners	-	40	40	40	40	40	-	-	-	200
Total	92	92	132	132	132	132	132	92	52	988

module has its strips aligned in the radial direction (ϕ-orientation) of the ATLAS co-ordinate system. The other module side is rotated ± 40 mrad depending on which disc it belongs to. There are two types of module rotations, which consequently result in two types of SCT layers: u and v.

- **u layer**: The wafers on the side closest to the beam have strips perpendicular to the beam (Φ wafers). The side which is furthest from the beam is rotated anti-clockwise with respect to the Φ wafers by 40 mrad.

- **v layer**: The wafers which lie on the side furthest away from the beam are perpendicular to the beam. The wafers opposite are rotated clockwise with respect to the Φ wafers by 40 mrad.

The u and v layers are alternated at each disc. Odd numbered discs have u-layers and even numbered discs have v-layers. The discs are positioned to provide a minimum of 4 space points per track. Disc one is closest to the interaction point.

5.1.3 Cooling and Environmental Gas System

Each module will dissipate up to 8 W of heat during the running of the detector. Approximately 6 W is due to the electronics and the remainder due to the leakage current which will increase as a result of radiation damage. In total up to 40 kW of heat needs to be removed once the SCT is irradiated. As a preventative measure for the reverse annealing of the SCT modules, each silicon wafer must be kept cool at a temperature below or equal to -7 °C. For this to be possible, a coolant temperature much lower than the module temperature is required. An evaporative cooling circuit was adopted giving many benefits:

- High heat transfer between cooling fluid and pipes;
- Small temperature gradient along cooling channels;
- Reduction in required material for cooling channels.

The choice of coolant is C_3F_8, it proves very stable against irradiation, is non-flammable, non-toxic and is electrically insulating. The basic concept of the system will be given, but for a more detailed description, please refer to [12].

The cooling system for the SCT and pixel systems is situated underground in the ATLAS cavern. There are four distribution racks, each one responsible for a single quadrant of the ID. Pressure regulators at these racks allow an absolute pressure between 11 and 15 bar to be set. This in turn delivers the liquid coolant at room temperature from the condenser along 30 m of thin copper tubing to the ID volume. Next, the liquid passes through a heat exchanger then very narrow capillaries, causing a pressure drop and a change from a liquid form to a bi-phase form. The fluid then boils along the cooling circuits within the SCT structure. Attached to small cooling blocks in contact with the cooling pipes are the detector

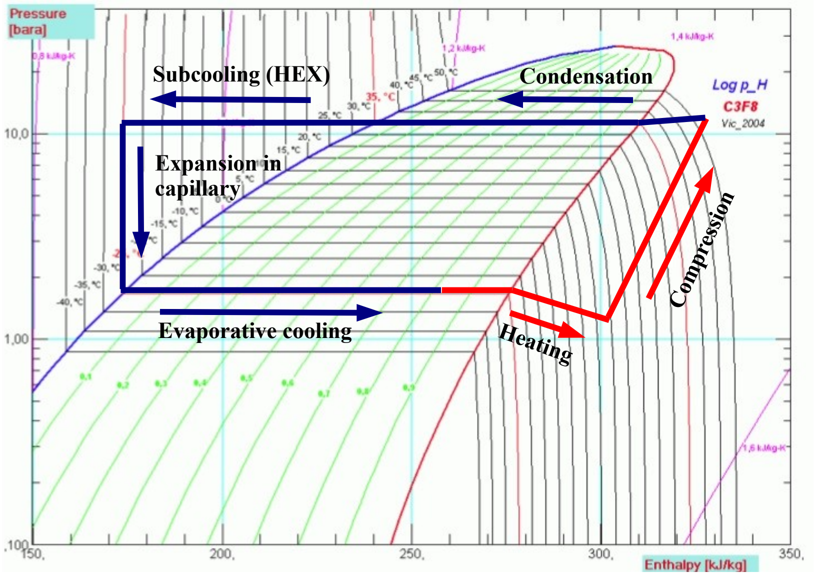


Figure 5.2: Log(p)-H diagram for C_3F_8*. On the x-axis is the enthalpy (kJ/kg) and the y-axis gives the pressure (bar absolute). A back pressure setting of 1.67 bar absolute ensures a -25 °C nominal operating temperature for the* C_3F_8*.*

modules. Their heat is absorbed and removed during this process. Any remaining liquid is boiled off in a heater just outside the endcap, which also raises the return gas temperature above the cavern dewpoint. Finally the gas is compressed, cooled and returned to the system in its original liquid form. A back-pressure regulator, situated also at the distribution racks, sets the required temperature of the coolant. This is 1.67 bar absolute, giving -25 °C for the normal operating temperature of the C_3F_8 (see Figure 5.2). As a result of the low operating temperatures for the coolant, it is essential that the moisture levels within the SCT volume are kept at a level whereby condensation will not occur. If condensation was to form, water in the SCT components would cause catastrophic damage. A requirement of 350 ppm (parts per million) is set for the moisture level. For air at a temperature of 20 °C at 1 bar pressure and a relative humidity of 50 %, the moisture level is 11690 ppm. In order to reach such a low moisture level, dry Nitrogen (N_2) is flushed through the entire detector volume. The endcap volume is estimated at 1700 litres. With a relative humidity of 50 % it contains roughly 14.7 g of moisture, needing approximately 6000 l of dry N_2 in order for it to reach the specifications. A flow rate of one volume exchange per hour is the specification laid out by ATLAS.

5.1.4 Thermal Enclosures and Heater Pads

The SCT is operated at -7 °C in a N_2 environment. In contrast, the TRT operates at room temperature in a CO_2 gas system. For this reason thermal enclosures are necessary to provide a barrier between the two different sub-detectors. An inner and outer thermal enclosure (ITE, OTE) seal off the SCT structure, preserving its low temperature and low humidity environment. It prevents any condensation forming as a result of the much warmer TRT (20°C). At the same time, any possibility of the N_2 flowing into the TRT and affecting its gas-gain performance is avoided. It is also a preventative measure against the CO_2 from the ID volume flowing into the SCT detector.

Attached to the OTE at the interface between the two sub-detectors, are heater pads, made from copper polyimide. This is to avoid build-up of condensation, by maintaining the external temperature above the dew point. The desired temperature is achieved by cycling the heater on and off at a rate of the order of 1 Hz. Each heater circuit is capable of providing between 150 W/m^2 - 300 W/m^2 (depending on its position on the OTE).

5.1.5 Grounding and Shielding

The objective of a grounding and shielding configuration is to minimise the flow of externally induced currents in the small-signal path of the SCT/Pixel detectors. For the SCT detector, the small signal path includes the detector strip, detector back-plane, module backplane capacitor, module front analogue ground bus, the small signal ground bus in the front chip, the first transistor in the amplifier channel, and the two chip bond wires for signal and ground [71]. The thermal enclosures, described previously, act as a Faraday cage, shielding the SCT from any external electronic noise pick-up. Without going into too much detail of the actual grounding connections, the idea behind them is simple. Any non-current carrying conductors are connected to a low impedance path to ground. In simplified form, each disc/barrel element (cooling pipes, power cables, hybrids, discs) is linked up to the support structure, which in turn is connected to the OTE. The OTE is the main path to ground away from the SCT detector. Eventually being connected to the ID Ground and finally the common ATLAS ground.

5.1.6 Material

By using the information known to us about the composition of the SCT, it is possible to provide an estimate of the radiation length in each component. *Bremsstrahlung* and *pair production* are the processes by which high energy electrons and photons lose energy. The scaling variable X_0 is the characteristic length (thickness of a material) over which the electron has reduced its energy by a factor e and for a photon, $\frac{7}{9}$ of its mean free path. A simulation using GEANT 4 [5] has enabled an estimate of the radiation lengths for the SCT components. Figure 5.3 gives a break-down of the different components in the SCT endcaps in radiation lengths.

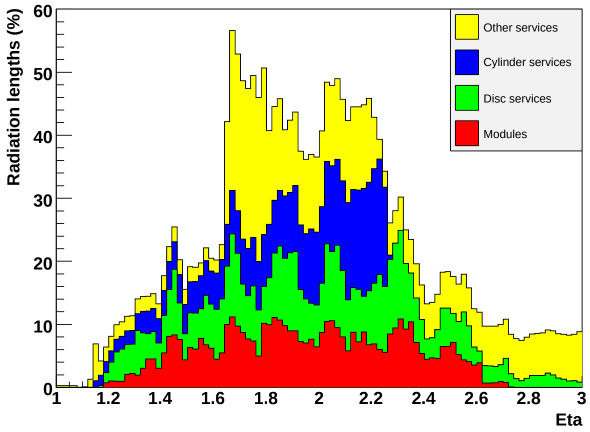


Figure 5.3: Mean number of radiation lengths traversed by a particle as a function of pseudorapidity originating from the IP for the SCT endcaps

5.2 Construction of Endcap-A at Nikhef

The next sections aim to guide the reader through the various steps undergone in constructing and testing endcap-A. A description of the tests carried out at Nikhef and CERN is given, leading to the next chapter which will describe the performance and test results of the detector.

5.2.1 Disc preparation

The bare disc was manufactured by an external company before being sent to Nikhef for dressing of the services. It consists of a carbon fibre sandwich with a Korex® honeycomb filling approximately 1.2 cm thick. These materials were chosen for their cost and physical stability. At Nikhef the geometrical tolerances of the bare discs were accessed, using a co-ordinate measuring machine (CMM). The specifications required a flatness of 300 μm accuracy. In reality the average flatness was better than 100 μm [2]. The discs were also tested that they were within specifications for stiffness, weight and resonant frequency. Next, the discs were placed in a support frame and using a reference mask, the printed pattern of required holes and apertures was machined in each disc. Then followed

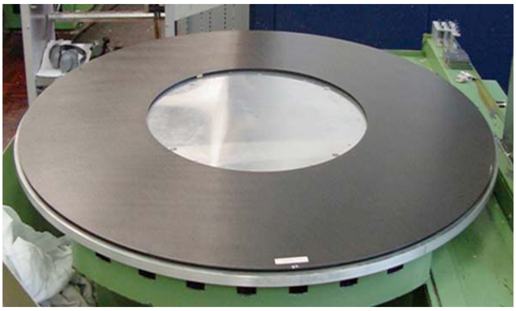


Figure 5.4: A bare endcap disc

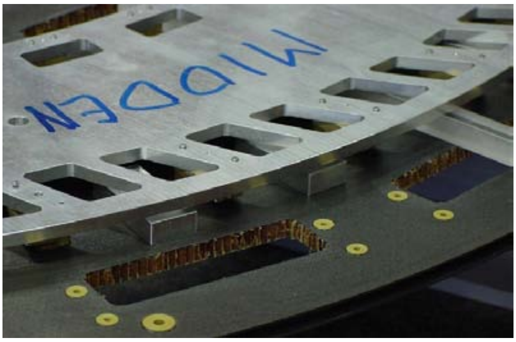


Figure 5.5: A reference mask for cutting the apertures on a bare disc.

Figure 5.6: A disc with holes for the services as well as cooling circuit mounts.

the inserts and pads necessary for the attachment of the cooling circuits. The pad surfaces were machined flat ensure that when the modules were mounted, they would be parallel to the disc. A tolerance of 50 μm was allowed for the inserts (see Figures 5.4 - 5.6).

5.2.2 Services to Disc

The next stage involves the attachment of the necessary services for the readout of the modules. These include, cooling circuits to keep the module temperatures optimal, power tapes for supplying the electrical power to the modules, optical ribbons for the TTC and data transmission, as well as various other services for the detector monitoring and alignment. All of the services reach the disc edge, where the interface between the cylinder and disc is referred to as PPF0. Each component will now be summarised.

Power tapes

Also known as wiggly tapes, these power tapes are made from Cu-polyimide and supply the control signal and high voltages to each module. They also have copper-clad twisted-pair conductors to supply low voltage power. Each wiggly tape can supply power for up to three modules. They are highly flexible to facilitate the easy routing between modules.

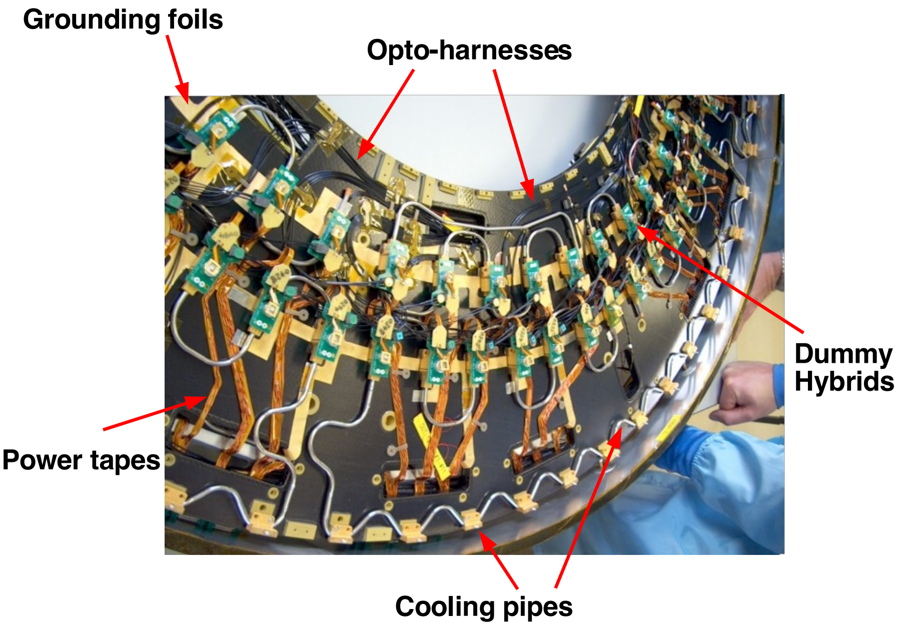


Figure 5.7: The front-side of a disc showing the various service components, including the cooling circuits, cooling blocks, optical fibres and wiggly tapes.

Opto-harnesses

Described more extensively in section 4.2.1, each opto-harness is capable of reading out up to six modules. There are two optical fibres for the receiving of data from the module and one transmission line to send the timing, trigger and control signals to each module.

Cooling circuits

The cooling circuits are highly modular allowing one circuit per disc quadrant. They have a Cu-Ni composition and consist of consecutive S-bends to alleviate the stress caused by thermal expansion. For the outer and middle circuits, both module ends are cooled. Whereas for the inner circuits, where the modules only consist of two silicon wafers (as opposed to four), only one cooling contact is implemented.

Cooling blocks attach onto the circuits. A peek split separates the block into two parts: a larger part for cooling the hybrid and a smaller one making contact with the spine for the removal of heat from the sensor. In each disc quadrant, the exhausts from the cooling circuits are output at the PPF0 disc edge. This results in up to 33 modules (13 outers and 10 middle and inners) being supplied by the same coolant line.

DCS sensors

Sensors for measuring the temperature and humidity of the discs and support structure and services are attached at various locations throughout the SCT volume. Up to 30 thermistors are positioned on one disc. See references [4] and [68] for more details.

FSI jewels

Frequency Scanning Interferometry (FSI) is a method used to make precise absolute distance measurements in a certain environment. Many such distance measurements can be made simultaneously. An interferometer exists for every distance that is to be measured. A laser is connected to all the interferometers in the system, and by scanning its frequency, the returned optical path for each interferometer in the system is compared to the path of a reference interferometer. The fringe cycles produced correspond to a constant phase difference. This phase difference is compared to the reference phase and the length of the path for each interferometer can be determined.

In the SCT, each section (barrel or endcaps) is monitored for any changes in shape. An FSI geodetic grid is implemented using 842 grid-line interferometers (GLIs), with 165 GLIs in each endcap. A quill/retro-reflector pair forms each GLI and are called "jewels". They are mounted onto the carbon fibre discs, with typically three jewels on the outer disc radius and 3-6 on the inner radius. On one side, is a quill which is attached to a glass beam splitter and a fibre ribbon. Infrared light is sent via the transmission fibre to the opposite retro reflector and the light signal sent back along the return fibre. Interferometric distances exist on points on each disc as well as points between discs. This way any changes in shape can be detected. The optical ribbons for the FSI run all the way back to the electromagnetic calorimeter cryostat walls, without any fibre splits. The fibres are then spliced to a multi-fibre ribbon and routed to the back of a readout crate. In this way, any loss of light is minimised [39],[41],[40].

Patch panels

A number of patch panels (Patch Panel Forward 0, PPF0) exist on each disc, located on the rear side at the outer edge (for disc 9 they are located on the front side as a result of its 180 degree front-back rotation). They enable the routing and positioning of the services necessary for the readout of the module and detector control system. On each quadrant there are four patch panels for the electrical services, two for the optical communication readout and one for the DCS system.

Grounding panels

Grounding foils are placed on the front and back sides of each disc to ensure proper grounding connections to all the applied services.

5.2.3 Testing of Disc Services

After the completion of the services to disc, several quality control checks were implemented before modules could be mounted onto discs. A mixture of both visual inspections and hands on measurements were performed on all the services. The visual checks included an inspection of the DCS temperature and humidity sensors, verifying that they were glued onto the correct locations on the cooling pipes and disc. Next, the FSI jewels and fibres were checked for any signs of damage. The cooling lines were checked for any defects in the routings or connections. Finally, a series of resistance measurements were performed on the grounding foils to check the quality of the grounding connections. Dummy hybrids and modules were built to allow the testing of certain services without the need for endangering any real detector modules. They allowed a heat load to be generated on the cooling circuit components as well as allowing a check of the HV and LV power lines. After the completion of services, the dummy hybrids or modules were mounted onto an entire disc which was then transferred to the disc test box for further tests.

Nikhef Test Setup and Programme

At Nikhef in 2005 a test-box was constructed for the testing of each SCT disc and their services. Located in the clean room at Nikhef, the box contained a mini-cylinder structure for supporting each disc and was connected to an evaporative cooling system as well as being equipped with optical readout fibres, power and DCS cables. The cooling system used a C_3F_8 coolant, the same as will be used during the ATLAS running. However, the design mechanism to cool the C_3F_8 was different from the standard ATLAS evaporative cooling system. Nikhef used a two stage cooling system, using R404A (an ozone friendly refrigerant) as the primary coolant and C_3F_8 as the secondary coolant. The temperature of the C_3F_8 could be regulated with the evaporative pressure of the R404A. This system did not need the oil-free compressor as utilised in the standard ATLAS evaporative cooling system. A detector control project created at Nikhef was designed to monitor various aspects of the test-box system as well as the surrounding environment. For testing the electrical functionality of the modules, the general SctRodDaq software and hardware set-up was implemented, as described in chapter 4. This next section gives a brief overview of each test used to verify the quality of the services. If any of the services failed during the testing procedure, they were either repaired or replaced before being retested once again for quality assurance.

Wiggly tape test: This test was performed to check for any discontinuity or short in the power cable. A second test, called the "snake test" checked the stability of the cable. The cable was rocked into different positions and the resistances in the power lines measured. Either dummy modules or hybrids were sufficient for this test.

Opto-harness and plug-in tests: Using dummy modules or hybrids connected to the wiggly tapes, the opto-plugins were connected. The *p-i-n* diodes were tested for responsivity to light emitted by a laser source and the two *VCSELS* were tested for light output. A laser was induced with a 100 mA current and shone into the clock and command fibre. The *p-i-n* diode responsivity to this light was measured. The requirements for a PASS were 0.3A/W. The data fibres were tested by powering the *VCSELS* with 10 mA of current and measuring the output light source using a large area photo-diode (LAPD). Using the known calibration constant for the LAPD the optical power was computed. A specification of $\geq 300\ \mu W$ at 10 mA was set. The rejection rate of opto-harnesses was low with 20 failures in total.

Cooling leak checks: The cooling lines were pumped with N_2 to a pressure of 20 bar. During the initial 30 minutes any big leaks could be detected by a big drop in pressure. Once this check passed, the disc was left overnight for 12 hours and a final pressure reading recorded the next day.

Power lines and cooling: Using the dummy modules, the cooling blocks were checked that they were properly coupled to the cooling circuits. A bad solder connection caused the thermocouple mounted on the copper pad of the dummy module to give a high temperature reading. The other DCS sensors were also readout to verify that they were working. The HV and LV lines were powered and the corresponding analogue and digital currents checked to be correct. Also any broken sense lines were recorded.

Thermal cycling: Each disc was thermally cycled a minimum of three times between a temperature of -25$^{\circ}C$ and +20$^{\circ}C$. This was to ensure that the services would still function correctly after a fluctuation in temperature. After the thermal cycles the pin positions of the module mounts were measured on the CMM to check that their positions had not moved, as a result of the thermal expansion and contraction of the discs. The positions in the plane of all of the mounting pins relative to the reference holes in the disks were measured. This was achieved with a precision of 10 μm, providing initial estimates of the position of each module on a disc. The resultant mean offset for all modules was 56 $\pm$ 58 μm in Rϕ for Endcap-A [2].

5.2.4 Modules to discs

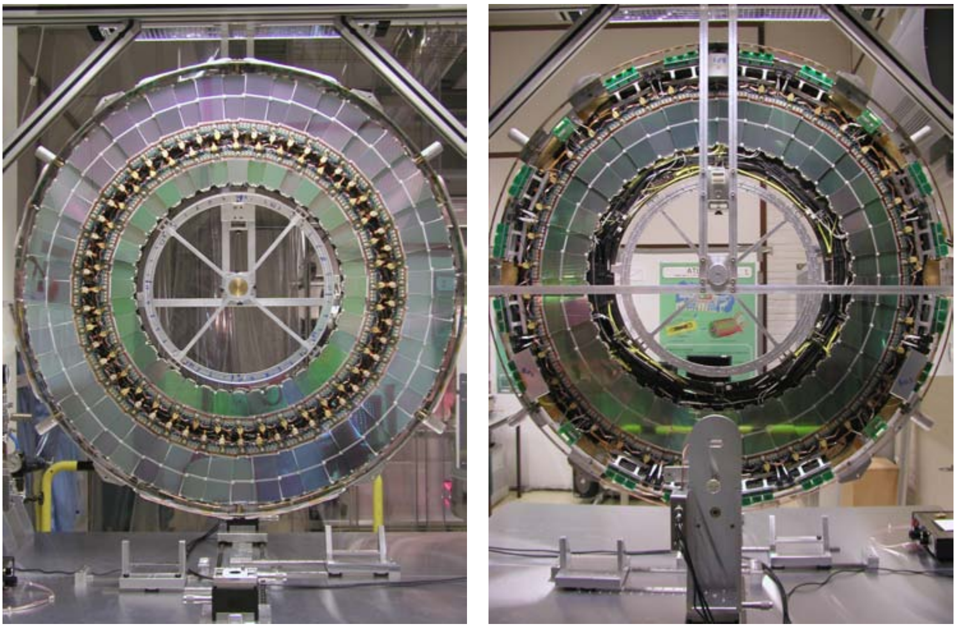


Figure 5.8: On the left is a photograph of the front side of Disc 6A after outer and inner module mounting and on the right, the rear side of Disc 6A with middles.

Nikhef received constructed modules from all the institutes participating in the production. Upon arrival each module was electrically verified that no damage had been caused as a result of transit. A full module characterisation sequence was performed which included testing of the digital and analogue functionalities. A handful of modules needed bonds to be repaired but then passed the characteristic sequence test afterwards. Once the quality of the modules was assured, the modules were ready to be mounted onto the discs. Disc 9 was the first disc to be installed into the cylinder, and was therefore the first disc to be fully populated with modules. A special test stand was used to hold the carbon fibre disc structure in place. Then using various tools, including a module grabber and transfer place the modules were mounted onto the discs. The lower modules were first installed, followed by the overlapping upper modules. To ensure optimal coupling to the cooling blocks, the module cooling pad was spread with a very fine layer of thermal grease.

Figure 5.8 shows the fully populated Disc 6A complete with inner, outer (front-side) and middle modules (back-side). Next, the fully populated disc was carefully mounted in the disc test box for further tests. The power, cooling, optical and DCS connections were established, followed by a test sequence similar to that described in 5.2.3.

The safety cover was placed over the entire disc once it was situated in the test-box. This was to avoid any passing damage whilst all the necessary connections were being made to the disc. The entire test-box was then sealed with a large panel, ensuring a gas and light tight set-up. The cooling lines were again filled with N_2 at 20 bar and left overnight to test for any leaks within the pipes. If the pipes were leak tight, the box was flushed with dry air for several hours to ensure that the dew point was low enough to be able to run the cooling, allowing the modules to be fully powered. Figure 5.9 shows a schematic describing the sequence of tests that each disc must pass before being installed in the endcap-cylinder. If any modules did not pass the electrical tests, then a replacement module was mounted in its place, and the tests re-run. Only a few modules had to be replaced in total. Approximately 23 working days were required for each disc to complete all of these steps.

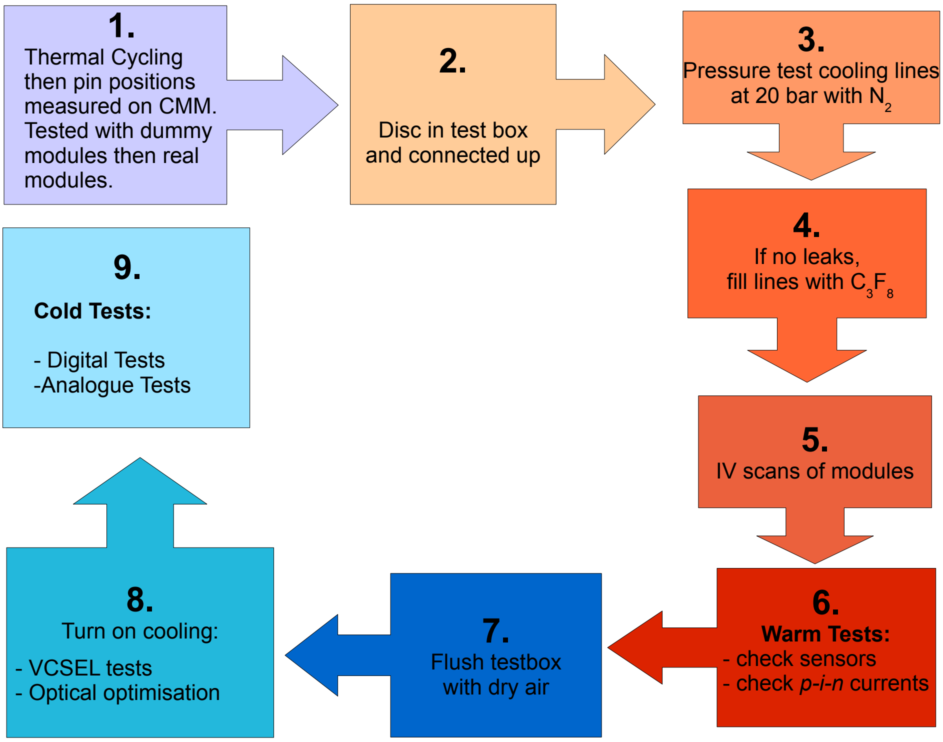


Figure 5.9: A flow chart of the various stages of tests in the disc test box.

5.2.5 Discs to cylinder

After the disc has passed all the necessary tests in the disc test box, it was installed in its final location in the endcap-cylinder. Special tooling was used to aid the installation of each disc. Two rails on a stable beam inside the inner-bore of the discs supported a trolley.

Figure 5.10: A disc held by the trolley on the supporting rails being inserted into its position within the cylinder support.

The trolley held the disc in place and a belt mechanism allowed the wheel to be glided into its nominal position. The tools were hand-operated during installation and three charge coupled device cameras were used to view the distance between the disc and the cylinder wall. Once the wheel was in position, and supported by the slots in the carbon fibre support cylinder, several screws fastened the disc securely in place.

A second test box (see Figure 5.11) was created for testing the discs in the cylinder. An insulating box was formed around the entire length and width of the endcap to maintain the environmental conditions needed during testing. A floor and top panel were permanently fixed, whilst side panels were made removeable. The panels were 100 mm thick, consisting of polyurethane, to give a sufficiently low inward heat leak. They were also covered on the inside and outside with aluminium to prevent moisture out-gassing and to act as a Faraday cage. The assembly frame acted as a clean face for fixing the panels, ensuring a gas, light tight, low-humidity environment. The panels had to be frequently removed to facilitate addition of services to cylinder, insertion of wheels, connection of cylinder services to wheels, alignment of wheels, as well as repair work. Additional cooling pipe extensions from the cooling plant to the cylinder were provided. The same optical test fibres and power cables from the disc test box were used. A dry air supply was also enabled to allow the air in the cylinder test box to be dried out. Various sensors were placed strategically around the cylinder box so that the environmental conditions could be monitored by the DCS project. The endcap has a large number of services, that emerge from the disc-9 end. In ATLAS these services attach to the liquid argon cryostat wall. The services are generally quite delicate since material is kept to a minimum to ensure minimal radiation length and volume. There are approximately, 1000 power tapes, 3000 optical fibres, 120 cooling pipes and several hundred DCS cables. In ATLAS the power tapes connect to a patch panel (PPF1). However, to minimise the usage and damage of the connectors to PPF1, a “Temporary Interconnect” cable (TI) was implemented which connected to a temporary patch panel (TPP) at the disc-9 end. They provided an interface to the test cables, attaching from PPF1 to the temporary patch panels. This test box was also designed to be used during transportation of the endcap to CERN as well as for further cold testing above the cavern in surface room 1 (SR1).

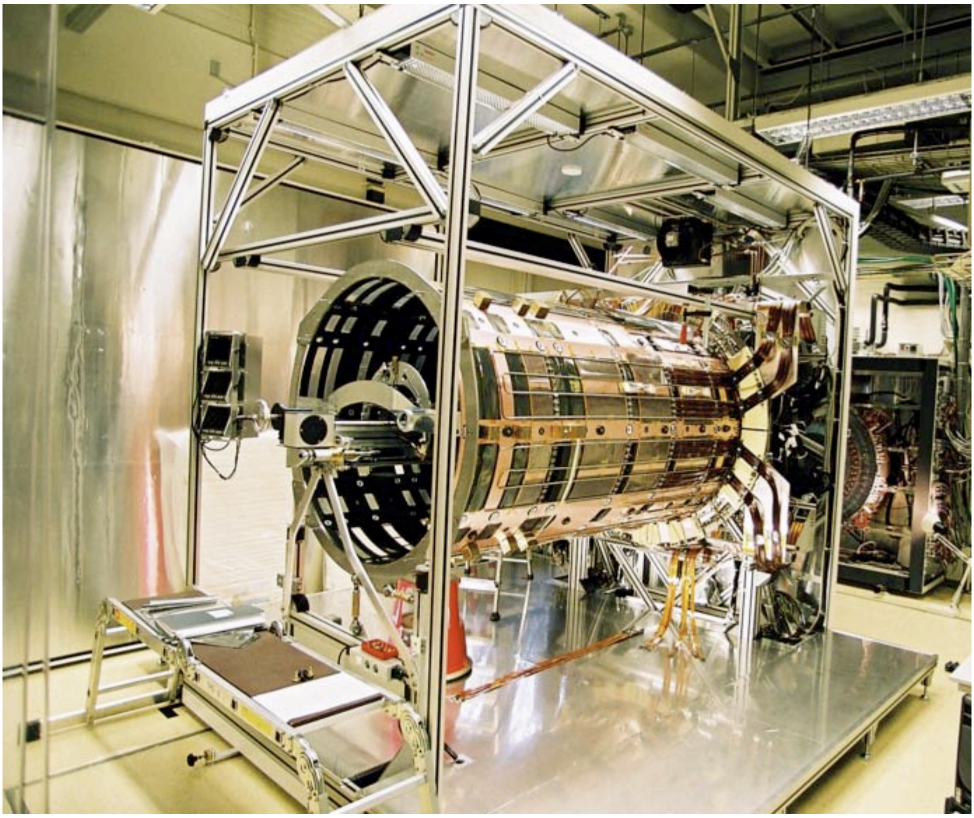


Figure 5.11: The Nikhef cylinder test box frame with the endcap support structure inside. The side panels have been removed. In the background, a part of the disc test box can also be seen.

5.2.6 Services to Cylinder

The cylinder support structure serves as the base for the routing of services between the discs and rear end of the endcap. The cooling pipes, power tapes, optical readout fibres and DCS components are all routed along the length of the cylinder. Here a short description of each is given.

The low mass tapes, serve as an extension to the previously described wiggly power tapes for the modules. They connect at PPF0 at the outer disc edge and run the entire length of the cylinder, terminating in cable trays at PPF1. The cables are laid in groups of 3 separate stacks comprising as many as 27 power tapes. There are up to 12 stacks in each quadrant. The cooling pipes connect at PPF0 to the capillaries which are routed along the cylinder to the edge of the support structure, exiting at the services thermal feedthrough (STFT). The flow in each circuit is kept the same by adjusting the capillary length. In addition to the module cooling, cooling pipe circuits for the low mass tapes are provided to minimise the amount of heat dissipated in he SCT volume. Each LMT tape stack is wrapped in foil, which in turn quickens the process for extracting the heat from the LMTs to the cooling pipes.

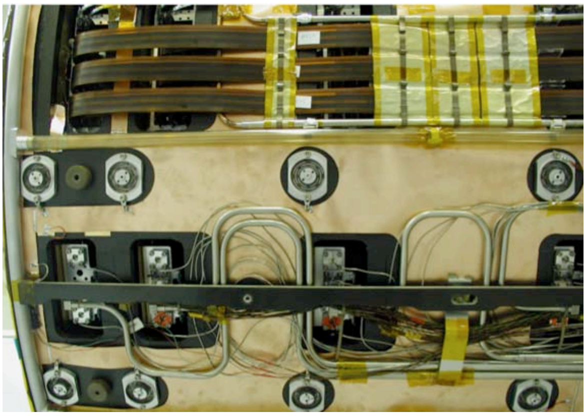


Figure 5.12: A photograph of the services attached to the cylinder support structure.

Optical ribbons connect at the PPF0 disc edge at an infinion junction which allows the on-disc opto-harness and on-cylinder fibres to fasten together securely. The fibres run along the length of the cylinder connecting to test fibres which are linked to the BOC readout cards.

Similarly, there are many DCS cables that connect at PPF0 to the DCS cables routed on the disc. These cables also connect at a further patch panel PPF1 where the final ATLAS DCS cables will eventually connect. In addition DCS humidity and temperature sensors are positioned along the cylinder in order to monitor the environmental conditions of the services and cylinder structure.

As each disc was installed in the cylinder, the various services necessary for the readout of the disc were tested. For the optical fibres, light was shone through the transmission fibre to the on-detector *p-i-n* diodes and a check to see that there was a reasonable current reading. For the *VCSEL*s, the power to the module was switched on very briefly for a few seconds and the receiver fibre checked for light output. This was performed safely by focusing the fibre on an infra-red wavelength shift card. Using the detector control system project, the various sensors were checked for functionality. Each of the on-cylinder cooling pipe circuits were checked for any leaks by pressure testing again with $\mathrm{N_2}$. If no leaks were found, the nitrogen was released into atmosphere and the cylinder was ready for the disc lines to be filled with $\mathrm{C_3F_8}$. Since it takes a number of hours to dry out the large volume of the cylinder test box, all of the service checks were performed first before closing up and sealing the side panels. Usually the test-box was left to dry overnight so that the dew-point was low enough for the cooling to be run at approximately a coolant temperature of -20$^\circ C$. Before switching on the cooling, all the relevant humidity and temperature sensors were checked first. Then the disc lines were filled with the cooled C_3F_8 . The optical communication was optimised using the RX threshold and delay scans, before commencing the analogue and digital tests. Appendix B provides an overview of the various tests performed.

5.2.7 Transportation from Nikhef to CERN

In April 2006, Endcap-A was ready to be transported to CERN for further testing as well as its final assembly and integration into the TRT. Simulations as well as a transport test were carried out to ensure that the endcap would not undergo any damage [70],[50]. The transport test used a dummy cylinder, representing the actual mass, size and positioning of the real endcap. Four shock loggers mounted with three displacement meters monitored the behaviour. A video camera of the test journey was also used to record the movement of the transport box. A lorry driven under normal conditions was used with a maximum allowed speed of 80 km/hr.

The cylinder test box was mounted onto a wheeled transport frame for ease of maneuvering during the loading and off-loading processes. The test-box was kept at a temperature below 35 °C and well below a limit of 80% relative humidity. The transport frame was attached to the testbox by wire-rope isolators, enabling a three dimensional shock absorption and damping. They protected against any minor bumps, minimising vibrations as well as a reducing the acceleration of the cylinder during both the journey and handling.

Using a large, removable window down to ground level in the Nikhef clean room, the complete test box and wheel frame was removed. It was loaded into an airbed suspension trailer with a controlled temperature and humidity. It was fastened securely for its 24 hr journey to CERN. Loggers were located in the trailer and on the endcap enclosure, recording temperature, shock and humidity. After the initial 30 minutes into the journey, the loggers were checked for any cause for concern before the continuation of the transportation.

5.3 Endcap-A at CERN

On arrival at CERN, several hours were needed to carefully off-load the endcap from the trailer, into its new location in the surface reception room 1 (SR1). A 600 m^2, class 2000 clean room area was set-up for the assembly of the pixel, SCT and TRT detectors. The endcaps were allocated a common working space where both endcaps could work in parallel to one another. A test set-up capable of reading out one full disc of modules at one time was assembled. This utilised the final design hardware and software components. This included three fully cabled PS crates and one ROD crate with three rods and corresponding fibres. An evaporative cooling system was setup for use in the SR1 test area for both the SCT and pixel detectors. There were three dedicated racks; one for the pixels, one for the SCT barrel and another for the SCT endcaps. In practice only two of the three racks were allowed to be in use at the one time. The back pressure of each rack could be set enabling each individual detector component to run tests at their required temperatures. With Endcap-A in its new test area at CERN, each of the discs had to be re-tested to check that there was no damage caused during transit. Keeping the temporary patch panels attached to the endcap cylinder frame, the modules for each disc were cabled up and retested. The usual test-sequence was performed, checking the cooling pipes for leaks before filling the lines with C_3F_8, ensuring that all the disc and cylinder sensors were functioning correctly as well as running a full electrical test sequence on the modules. These test sequences are referred to as reception tests.

5.3.1 Completion of Endcap-A

Once all the reception tests were performed, the final stages of the endcap were completed. In October 2006, the endcap was transferred from its test-box and supported at one end by a "cantilever stand". This allowed the addition of the inner and outer thermal enclosures to be inserted and sealed. Figure 5.13 shows a photograph of the OTE ready for installation on Endcap-A. The leak tightness of both were tested as well as the general functionality of the heaters attached to the OTE. A leak rate of 85 litres/hr at 1 mbar over-pressure was achieved for Endcap-A. Lastly, any final grounding and shielding connections were made between the thermal enclosures and the endcap cylinder structure.

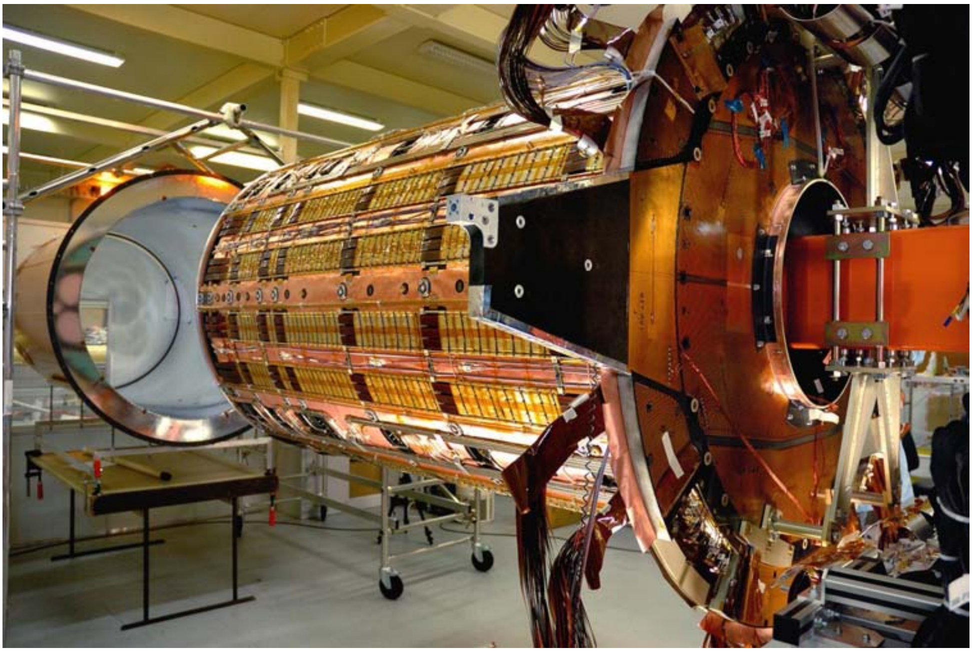


Figure 5.13: Outer thermal enclosure about to be installed on endcap-A located at SR1.

To check that there was no damage caused to the cylinder services during the insertion of the OTE, a second test stage was setup. One eighth of all the modules were fully cabled-up in order to be readout. Checks of the sensor, power and optical connections were first made, followed by a complete noise readout of this octant of modules. This checked that the grounding and shielding of the thermal enclosures was functioning correctly and that there was no increase in noise from the modules. Noise scans were also performed with the OTE heaters both ON and OFF and a check made for any crosstalk.

5.3.2 Integration with TRT and Final Installation

In November 2006 the completed Endcap-A was ready for integration with the TRT. The endcap remained on its cantilever stand, and was aligned to a set of rails which were fixed to the floor of the working area. The TRT had been mounted onto a special trolley which allowed it to roll over the SCT using the set of guide rails. The two structures were aligned using a frame fixed to the rails and a system of alignment wires. The final addition of the

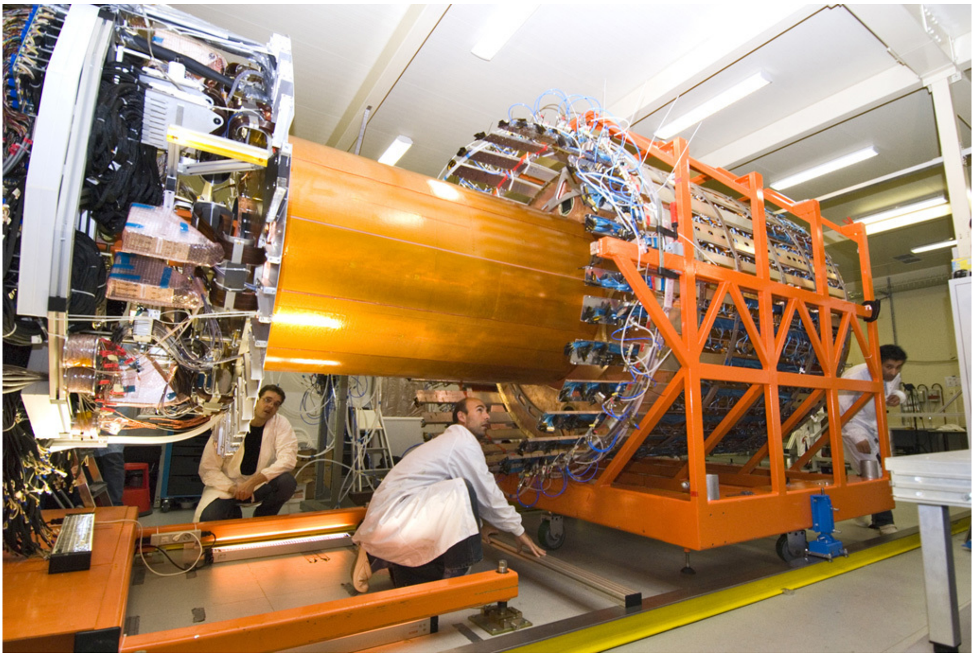


Figure 5.14: The integration of endcap-A TRT and SCT detectors in November 2006.

front and rear-end supports were added to complete the TRT/SCT Endcap-A. In May 2007, the complete unit was placed carefully into a box for transportation to the ATLAS surface building. Using special building cranes, the endcap was slowly lowered down the ATLAS shaft into the cavern to be positioned in line with the cryostat. It was carefully manoeuvred into its final resting place and the final connections and routings of the services begun.

During the cavern commissioning stages, the readout of the SCT and TRT were checked separately as well as being run together. A full characterisation of the modules was performed to ensure the functionality of all of the modules.

5.4 Cooling Problems

The inner detector evaporative cooling has had a history of problems since detector commissioning tests were performed at the beginning of 2007. Two major faults caused a significant loss of time to the inner detector test schedule. The first major fault involved the SCT heaters and the second was a fault with the external cooling plant.

5.4.1 Heaters

The first substantial tests of the combined evaporative cooling system was in February 2007 during Barrel testing. Part-way through the tests a short occurred within an electrical connector supplying the power to the heaters. The heaters are located downstream from the detector cooling loops. Their role is to boil away any remaining C_3F_8 liquid in the cooling pipes as well as raising the temperature of the gas above the cavern dew-point. It is a small heating element put into the inside of the cooling pipe at the exhaust. After an investigation, it appeared that moisture was creeping into the connector. Consequently, all heaters were

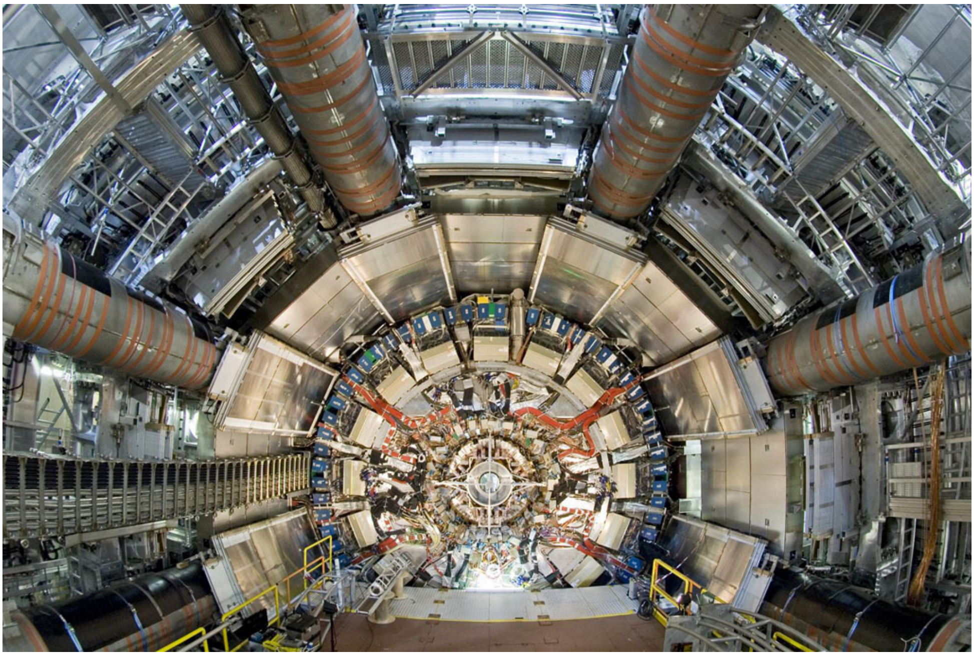


Figure 5.15: Final Installation of Inner detector Endcap-A completed on May 24^{th} *2007.*

removed and re-fitted with a sleeve to prevent any more moisture getting in. However, just before the endcaps were due to be installed in May, the same heater fault occurred. A new heater layout was introduced to allow future repairs of heaters at a more accessible location, as well as allowing the continuation of detector installation whilst a solution was found for the heater failures. Nearly 120 heaters were moved to a more serviceable area, from the cooling exhausts at the SCT detector to the back of the cryostat flange. New pipe work had to be re-engineered and then everything installed and leak tested. This re-work took until the end of 2007 to complete, allowing no cold testing of the SCT.

A solution has been made by re-designing the heater connector. The new designs have been installed and tested. Alternative heater designs are being investigated. A printed circuit instead of a coiled wire is one option, the other is a passive system that uses a hot liquid to heat up the cold C_3F_8 liquid from the detector. In addition, there were problems found with the heat exchangers, requiring more re-work. The connections were not leak tight and they all had to be removed, re-soldered, re-tested and installed and leak checked.

With both these solutions having been implemented, there have been no more faults, allowing the sign-off tests of both the barrel and endcaps to be finished.

5.4.2 Cooling Plant

After the sign-off tests of the barrel and endcap, the pixel commissioning was underway. In May 2008, subsequent cooling problems caused considerable delays to the schedule. Three out of six inner detector compressors failed catastrophically. The magnetic couplers slipped during the cooling start-up and were unable to drive the crank used to perform the compression. They also acted as a sealant of the C_3F_8 cooling volume from the motor and the compressor shaft. This caused the compressors to burn out as well as the loss of

100 kg of C_3F_8 from the system and the remaining 900 kg contaminated. Fortunately, only the cooling plant was affected and not the detector itself. A huge clean-up operation was implemented, involving the cleaning of the cooling plant as well as re-pairing of the compressors. The replacement of dirty pipe work was also necessary and additional filters were put in place.

The actual cause of this coupling slippage is still unknown, since an incomplete logging of data has made it difficult to come to an exact conclusion. However, sensors have been added to the system to detect any future slippage of the couplers. A C_3F_8 recovery tank has also been installed and tested, preventing any further losses in cooling liquid. Since then, the pipe work has been leak tested, new C_3F_8 has been introduced into the system and a successful commissioning of the cooling plant has been made. The pixel b-layer was cooled successfully during the ATLAS beam-pipe bake out, with the centre of the beam pipe reaching 220°C. Better monitoring and logging of the cooling system will ensure a better understanding of the future replication of a fault.

The next chapter will now give a summary of the performance of endcap-A. The results are based on the tests taken at both Nikhef and CERN over the two years of production, construction and installation.

CHAPTER 6

ENDCAP-A: PERFORMANCE AND TEST RESULTS

"If we knew what it was we were doing, it would not be called research, would it ?"

Albert Einstein.

Contents

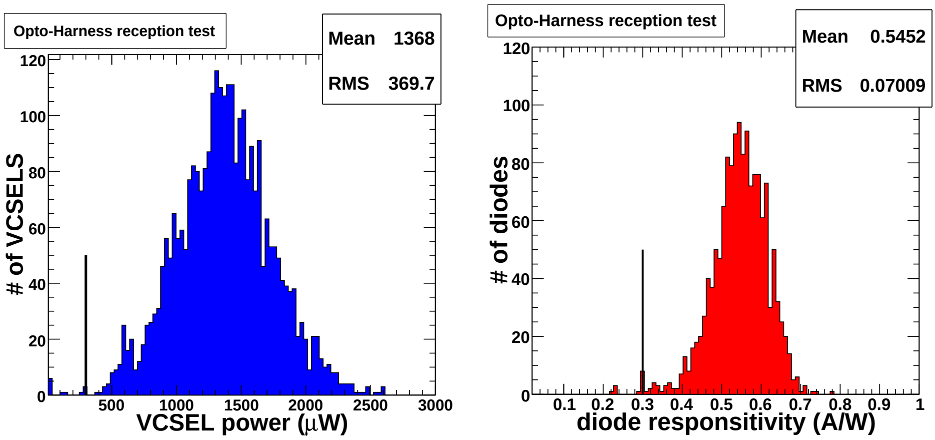
In this chapter, the results from various stages of test sequences will be summarised. This includes tests taken in the disc and cylinder test boxes at Nikhef, reception tests at CERN and most recently, the tests taken in the ATLAS cavern. The overall performance will be compared to the specifications as set out by ATLAS.

6.1 Optical Links

As mentioned earlier in chapter 4 optical links are used to communicate with the modules. The entire SCT system uses 8176 data links and 4088 transmission links. They have undergone various tests to ensure that they meet the requirements set out by the SCT community. This includes checking the individual harnesses before and after being put on each endcap-disc as well as frequent tests performed throughout the various stages of module testing. It is also an important factor that the links can work over a wide range of settings. Single bit errors as well as random hits will cause a loss in the number of real hits being read out. An upper limit of 10^{-9} for the bit error rate is set in order to maintain a high level of working efficiency for the optical links.

6.1.1 Harness and Disc tests

As described in section 4.2, the opto-harness includes the connector, *VCSEL*, *p-i-n* and fibre. On reception of the opto-harnesses at Nikhef, a number of tests were performed to check that there was no damage caused in transit. These tests checked the performance of both the *VCSEL* and *p-i-n*s. A series of bit error rate measurements were taken for each *p-i-n* on each endcap-harness. The set-up used six *VCSEL*s, one for each *p-i-n*. Each *DAC* unit equates to 10 mV which is used to determine the output current of the *VCSEL*. The TX *DAC* current setting ranges from 0 - 255, corresponding to approximately 0 - 18 mA. 32 kbits of pseudo-random data were sent to each on-detector *p-i-n* and the data returned checked against the reference sent data. Any differences were counted as errors. This scan was performed for each TX *DAC* value, giving the working range of the link, where no errors were returned. During the test, the *p-i-n* was biased at 6.1 V. At the end of the test, the responsivity of the *p-i-n* was calculated, measuring the current induced across the *p-i-n* for a known light output shone onto it. Similarly, the *VCSEL* performance was tested by powering each *VCSEL* at 10 mA and making a bit error rate test as a function of RX *DAC*. Again, 32 kbit of pseudo-random data was sent and the received data sent back was checked for errors. The threshold at which the receiving of a hit (or 1) of data was defined by the RX *DAC* setting. The maximum *DAC* value minus the minimum *DAC* value for which there were no errors was taken to be the working range of the *VCSEL*. An RX *DAC* setting of 255 is equivalent to approximately 255 μW of power. Using a calibrated large area photodiode, the power of each *VCSEL* at 10 mA setting was measured. Figure 6.1 shows the distributions of the *p-i-n* responsivities and *VCSEL* powers. A *VCSEL* power of less than 300 μW and a diode responsivity less than 0.3 A/W was regarded as a fail.



(a) (b)

Figure 6.1: Figure (a) shows the VCSEL powers (corrected for 50% duty cycle) of the reception tested opto-harnesses with a cut at 300 μW. On the right (b), the calculated diode responsivities with a cut at 0.3 A/W.

If the harness passed the criteria then it was mounted onto a disc and re-tested using

Table 6.1: A comparison of the pre and post disc assembly tests of the optical harnesses. The table gives the average value of all harnesses and the rms spread.

Test stage	*VCSEL* power @ 10 mA (μW)	Diode Response (A/W)
Pre-disc assembly	1368 ± 369	0.545 ± 0.070
Post-disc assembly	1183 ± 349	0.506 ± 0.065

dummy hybrids to check for any damage as a result of the routing of the harness on the disc. Table 6.1 gives a summary of the results for the *VCSEL* power and diode responsivities at both pre and post harness assembly onto discs. The results for pre and post assembly are comparable. The post assembly values are slightly lower which are most likely due to the two different measurement set-ups. Once the modules were mounted onto the disc, the exact responsivities were no longer measured. Instead values of the *p-i-n* currents were monitored and recorded by the SctRodDaq software. The level of the *p-i-n* currents gives a good indication of whether or not the diodes will function optimally. Typically, when there is no light shone directly onto the diodes, a value of 0.03 mA is still recorded by the software. The default setting of 160 for the TX *DAC*, gives induced *p-i-n* currents ranging from 0 - 0.8 mA. After the endcap was in its final position in the ATLAS cavern, the *p-i-n* diodes were re-tested to check that there were no breakages in the long (≈100 m) optical fibre, that was transmitting the light. Figure 6.2 shows the distribution of the *p-i-n* currents for Endcap A. The high number of *p-i-ns* at zero current were due to electro-static discharge damage of the off detector *VCSELs* at the back of crate cards. Over the course of testing, the failure rate for these *VCSELs* was very high with at least one VCSEL death per day. The electro-static discharge damage was traced back to an un-grounded soldering iron at the manufacturer, which was used when inserting the *VCSELS* into the plug-ins. A new batch of *VCSELs* have been ordered and will be replaced. Only one *p-i-n* on Endcap-A was actually lost. This was most likely as a result of a breakage within the optical fibre. Using the redundancy link, this module received its clock and command signals from its neighbour.

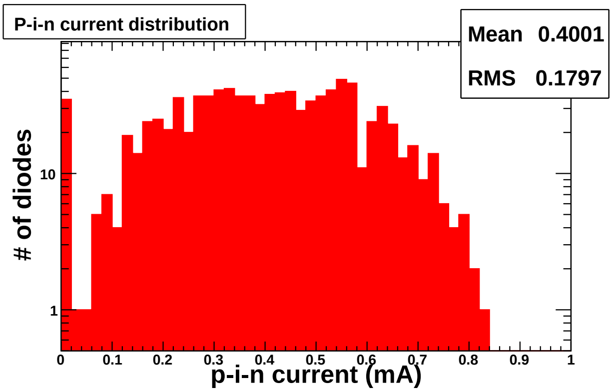


Figure 6.2: The p-i-n diode currents measured during the fibre sign-off tests in the ATLAS cavern for Endcap-A.

The next important step in the optimisation of the optical links is defining the correct receiver thresholds for the RX links which send the data from the module to the off-detector hardware. This will now be discussed.

6.1.2 RX Optimisation

The receiving end of the data acquisition is formed by the 'RX link'. Its task is to decode the light signal sent by the *VCSEL* on each module. Each link needs to have the receiver threshold correctly set so that there will be no loss in valid hits from the detector. The working range for each module is determined and the best threshold setting found for optimal communication. The RX optimisation is performed at the beginning of a test sequence. To establish module communication the decoding has to be calibrated. During this calibration three categories of problems can be recognised:

Slow turn-off: The black background is due to the slow turn off for the silicon *p-i-n* diodes that receive the light at the BOC. Problems can arise when the background is very high and the working range of the link already small. Then, a suitable setting may be difficult to find. A decrease in the *VCSEL* voltage should help lower the BOC *p-i-n* diode saturation and give a wider working range for this link.

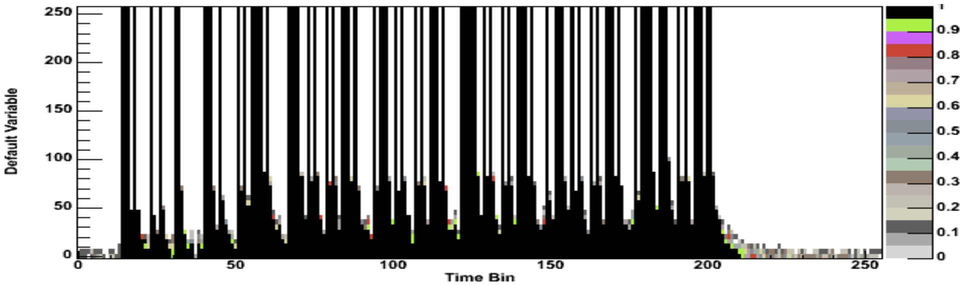


Figure 6.3: Link 0 of 4A-BR-O11. A reduction in the VCSEL voltage setting could reduce this slow turn-off effect.

Slow turn-on: This is due to the *VCSEL* needing a longer time than normal to switch on fully. Its light output increases significantly at the start of a burst of data. This phenomena is specific for a *VCSEL* and is partially understood [24]. This allows only a small working range for this link. In some cases, an increase in *VCSEL* voltage can help remedy this problem.

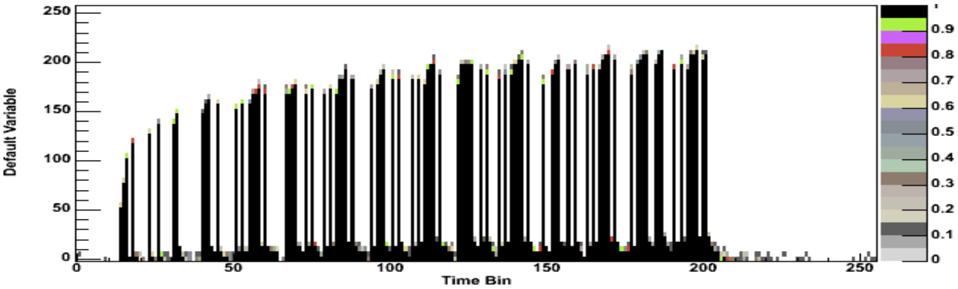


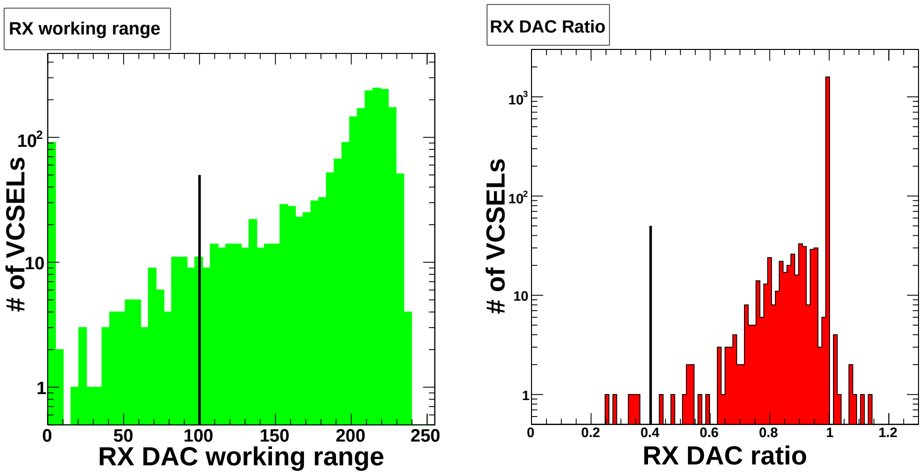
Figure 6.4: Link 1 of 4A-BR-O11. An increase in VCSEL voltage would improve link 1.

Low light: When there is not enough light emitted from the on-detector *VCSEL*, the threshold for the receiver must be set much lower. Sometimes it helps to increase the *VCSEL* voltage.

Figures 6.3 and 6.4 show an example of a problematic module where both its links suffer from one of the categorical problems. Link 0 in the upper plot could be improved by turning down the *VCSEL* voltage. However, since both links are determined by the same voltage setting, link 1 (lower plot) would most probably stop working. In such a case, the better working link can be configured to readout the data on both sides of the module, leaving the other link off.

An analysis of the optical link performance was performed by calculating the working range of each link, defined by finding the minimum and maximum threshold. The difference is called the working range (RX DAC) and is plotted in Figure 6.5a. The majority of the optical links have a healthy working range around 200. For the links that have a range less than 100, finding a more suitable threshold can be more difficult.

Many *VCSEL*s suffer from a mild form of slow turn-on, therefore a study was performed to determine the links which were too critical to use. Using the threshold scan, a plot was made of the ratio of the amplitude of the first pulse in the train to the last pulse in the train. Figure 6.5 gives the results. A healthy link will have the same threshold value set for both the first and last pulse trains, thus giving a ratio of 1. For links whereby the slow turn-on is extreme, a much smaller ratio will be calculated. A cut of 0.4 was made on the RX *DAC* ratio. Links with a ratio less than this cut were classed as critical and should always be switched off. There were a few links with an intermediate level of slow turn-on (0.4 - 0.6), which should be used if at all possible. We are not confident in the reliability of the *VCSEL*s therefore we want to keep the possibility of using the redundancy system for as long as possible. In the future, the SctRodDaq should be more tolerant to low bit error rate which might enable the recovery of a few of these problematic channels.



(a) (b)

Figure 6.5: (a) shows the working RX DAC range of the VCSELs for Endcap-A. (b) gives the ratio of the maximum DAC values of the first and last pulses in the train. A cut at 0.4 denotes critical VCSELs which are difficult to set a threshold making them use-able.

To summarise, 98.7% of the receiver links were operational at the time of installation. Table 6.2 gives an overview of the most problematic links for Endcap-A. In addition, there was one *p-i-n* diode with no response for module in position 5A-TR-08. This module, therefore, is set to redundant mode, enabling the receiving of clock and command signals from its neighbour. Another module (4A-TR-O10) had an unusual *p-i-n*-diode response. When there was no light induced on the diode a value of 0.83 μA was measured, when typically it should only be 0.04 μA. This effect did not affect the performance of the optical link.

Problem	Found at	Module	Link
Dead	CERN	2A-TR-O12	L1
Dead	Nikhef	2A-TR-I1	L1
Dead	CERN	2A-TR-I4	L1
Dead	Nikhef	2A-BR-M2	L0
Dead	CERN	2A-TL-O4	L1
Dead	CERN	4A-TR-O13	L0
Dead	Nikhef	5A-TR-O10	L0
Dead	Nikhef	5A-BL-M5	L1
Dead	Nikhef	5A-TL-M6	L1
Dead	Nikhef	6A-BR-M1	L0
Dead	Nikhef	6A-BL-M9	L0
Dead	Nikhef	6A-TL-M6	L0
Dead	CERN	8A-TR-M8	L1
Dead	Nikhef	9A-BL-O8	L0
Dead	CERN	9A-TL-O10	L0
Critical slow turn-on	Nikhef	1A-BR-O3	L0
Critical slow turn-on	Nikhef	3A-TR-O8	L1
Critical slow turn-on	Nikhef	4A-TR-O10	L1
Critical slow turn-on	Nikhef	4A-BR-O11	L1
Critical slow turn-on	Nikhef	5A-BR-M4	L1
Low light	Nikhef	4A-TR-O12	L0
Low light	Nikhef	9A-TL-O11	L1
Test crasher	CERN	1A-BR-M6	L0 (Chip M0)
Slow turn-off	Nikhef	1A-BL-M7	L0
Slow turn-off	Nikhef	6A-TL-M2	L1

Table 6.2: A summary of the most problematic RX optical links.

6.2 Power dissipation and Cooling

At all stages of the module testing, an archive was made recording the various module attributes and their environment variables. This included all current, voltage and temperature readings both on the modules, the discs, cylinder and surrounding test boxes.

6.2.1 Leakage Currents

At LHC start-up the nominal operating voltage is expected to be 150 V. On average the depletion voltage is around 80 V. Previously mentioned in chapter 3, the module sensors were manufactured by both Hamamatsu and CiS. Most modules behave like diodes and show standard I-V characteristics. The CiS modules have a different layout of the surface layer. As a result the sensor may show breakdown in a dry environment, giving higher leakage currents. The total leakage current as a function of bias voltage can be described by:

$$I_l = \begin{cases} A \cdot \sqrt{V_{bias}} + B \cdot V_{bias} + C & V_{bias} \leq V_{dep} \\ A \cdot \sqrt{V_{dep}} + B \cdot V_{bias} + C & V_{bias} > V_{dep} \end{cases} \tag{6.2}$$

where A, B, C are constants. The first term describes the contribution due to the charge generation current. It is proportional to the volume of the depletion layer and therefore is proportional to the bias voltage which controls this depletion zone. At full depletion, this term is kept constant. The second term describes the contribution due to the surface current. This current is assumed to behave as a current through an ohmic resistor. The last term is introduced to absorb any possible offsets in the readout measurement [57]. The surface current flows around the edges of the silicon module as well as through the SiO_2 and passivation layers. They are largely caused due to surface contaminations and can be humidity, temperature and time dependant.

The individual SCT sensors that make-up the modules had I-V scans performed on them. Only the wafers that passed the SCT specifications for leakage current were allowed to be formed into modules. For each module, several current-voltage (I-V) scans were taken to check that each module was within the specifications. The high voltage was ramped from 0 V up to 150 V and the current measured at 10 V intervals. This effectively changed the volume of the depletion zone. The specifications during tests allowed 6 μA at 150 V and up to 20 μA at 350 V. There were no modules that were rejected for high leakage currents during the qualification stages of testing. During the Nikhef assembly tests and CERN reception tests, the time between each 10 V step was very short during the module I-V scans. A more precise measurement was taken of all the modules, after installation of the endcap in the ATLAS cavern. The measurements were repeated several times allowing the current to settle, before it was ramped to the next voltage.

Figure 6.6 gives a summary of the leakage currents measured at 150 V during the reception testing at CERN. The CiS modules are on average much higher than Hamamatsu modules. Using equation 6.2 the I-V curves for the SCT modules were fitted. Figure 6.7 shows an I-V curve example for a CiS and Hamamatsu module. The depletion voltages were measured by the manufacturer and were fixed in the fits. The higher current behaviour of the CiS module (left) compared to the Hamamatsu module (right) is prominent. The results for the fits are not very precise since the leakage current monitoring at the low bias voltages (between 0 and 20 V) is not very sensitive in this region.

For the CiS modules which had early breakdown voltages it was possible to train them to operate within specifications in a dry environment. Figure 6.8 shows the CiS sensor behaviour during training [44]. Initially the sensor is placed in a dry environment ('RH curve') and the high voltage is ramped up to 150 V ('Vbias curve'). The 'Ibias' curve shows the bias current behaviour. The current rises steeply as the voltage is ramped up. With time in seconds on the x-axis, the current remains at 6 μA for over 30 minutes in the dry atmosphere. Next, the relative humidity is increased until it reaches 50%. The current discharge drops instantaneously. The environment is then switched back to being dry (0%) and the micro-discharge does not return. In this way the CiS sensors are fully use-able.

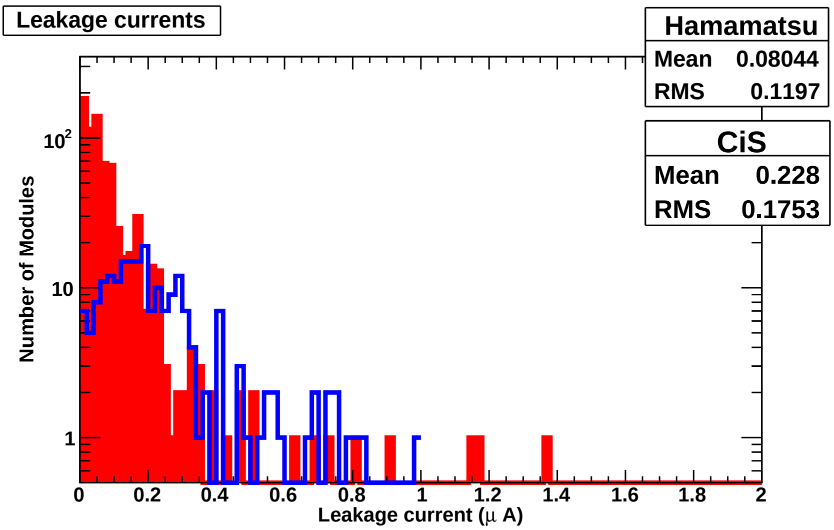
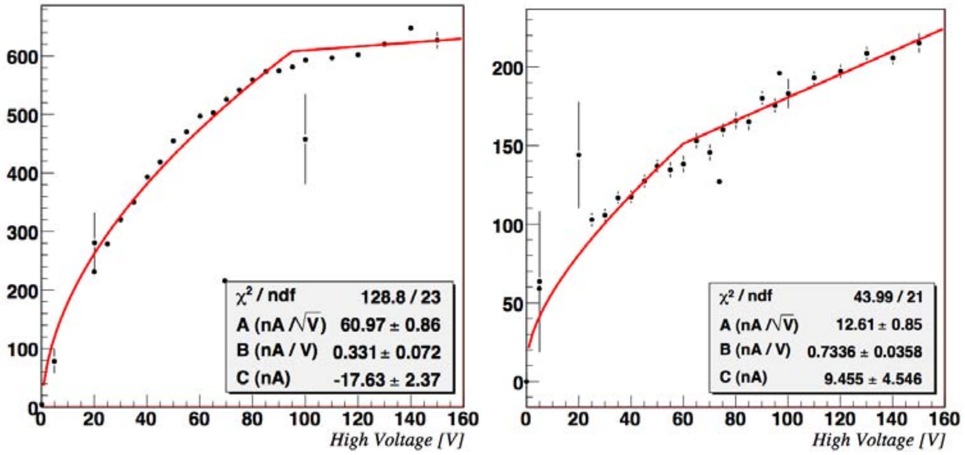


Figure 6.6: The leakage current distribution for Hamamatsu (solid colour) and CiS modules (bold line) on Endcap-A taken at a module temperature of 10 °C.



(a) (b)

Figure 6.7: I-V scans of two modules taken during commissioning tests in the ATLAS cavern. The x-axis gives the high voltage in volts, the y-axis represents the leakage current in nA. Figure (a) shows a CiS Module (6A-TL-I5) with $V_{dep} = 95$ V and (b) a Hamamatsu module (6A-TL-O1) with $V_{dep} = 60$ V.

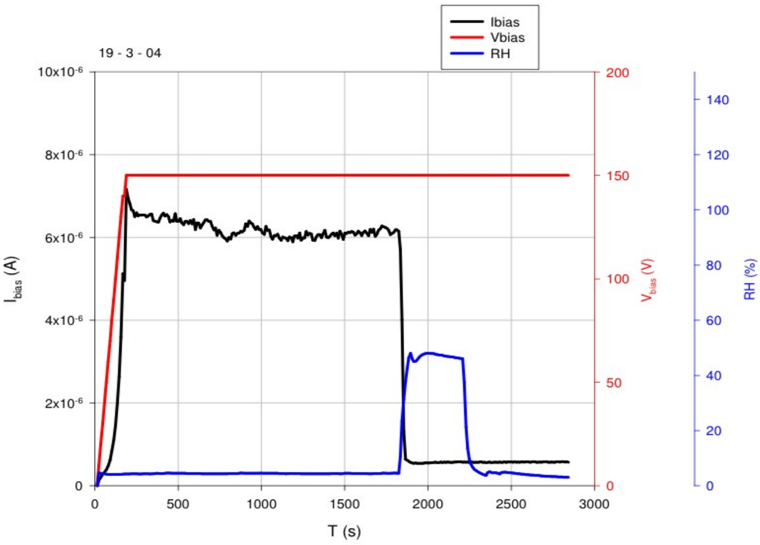


Figure 6.8: Training of a CiS module with micro-discharge. See text for details.

In the next section, the results for the various temperature readings will be discussed, beginning with the module temperatures.

6.2.2 Module Temperatures

The temperature of the hybrid was also monitored using a thermocouple placed directly on the hybrid surface. The connection of each module cooling block to the copper pipe circuit determines the quality of the module cooling. At Nikhef the modules were run at a coolant temperature of around -20 °C and a hybrid temperature approximately 20 °C higher. At CERN, the temperature of the coolant was between -10 and -5 °C.

Figure 6.9 shows an example of the distribution of module temperatures on disc-8 during tests at Nikhef. There is one outlier that needed its cooling block replaced and re-soldered, to give a better cooling connection. Figure 6.10 shows the spread in module temperatures during the reception tests at CERN. A summary in Table 6.3 gives the temperature spreads during all stages of testing.

Module type	Disc completion	Cylinder completion	CERN reception
	(°C)	(°C)	(°C)
Outers	3.62 ± 3.76	4.84 ± 2.16	13.86 ± 1.61
Middles	2.08 ± 2.78	4.24 ± 1.76	13.92 ± 1.86
Short Middles	6.15 ± 1.81	8.38 ± 1.43	14.30 ± 1.59
Inners	2.39 ± 2.00	4.76 ± 1.71	14.75 ± 1.66

Table 6.3: A summary of the mean hybrid temperature and spreads during various testing stages.

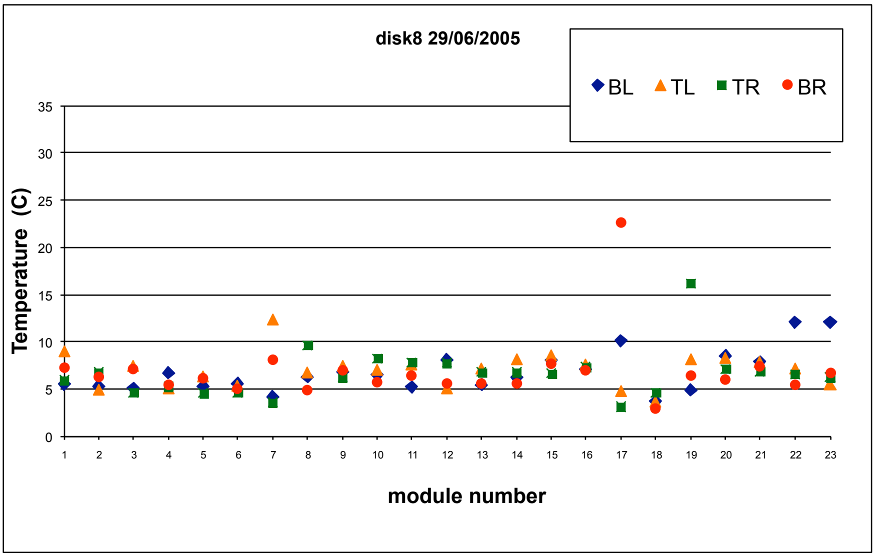


Figure 6.9: A distribution of the module hybrid cooling temperatures at Nikhef for disk-8. Any problems with the quality of the cooling block connection to the cooling pipe can be identified. Blue diamonds represent BL, orange triangles TL, green squares TR and red circles BR.

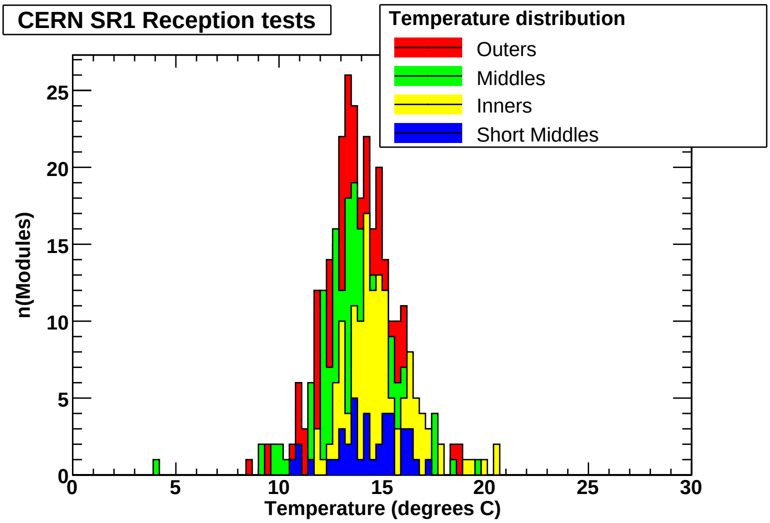


Figure 6.10: The hybrid temperature distribution for each module type –outer, middle, short-middle and inner – recorded during reception tests at CERN in SR1.

6.2.3 LMT Cooling

In each quadrant of the endcap cylinder there are four LMT bundles. One sided cooling reduces the amount of heat generated by the currents providing the power to the modules. There is cooling on either side of two LMT bundles, providing cooling to only one side of each LMT group. In order to monitor the effect of the cooling of the module power tapes, a thermocouple was attached to the upper middle LMT within the stack. (Ideally it should have been placed within the most central point of the stack but there was an error in the positioning of the thermocouple.) There were nine tapes in a 3 stack by 3 tape configuration. Another thermocouple was attached at the services thermal feed through end of the same stack of LMTs where there was no cooling. The coolant temperature was approximately 0 °C. The power to the modules was switched on and off in various cycles.

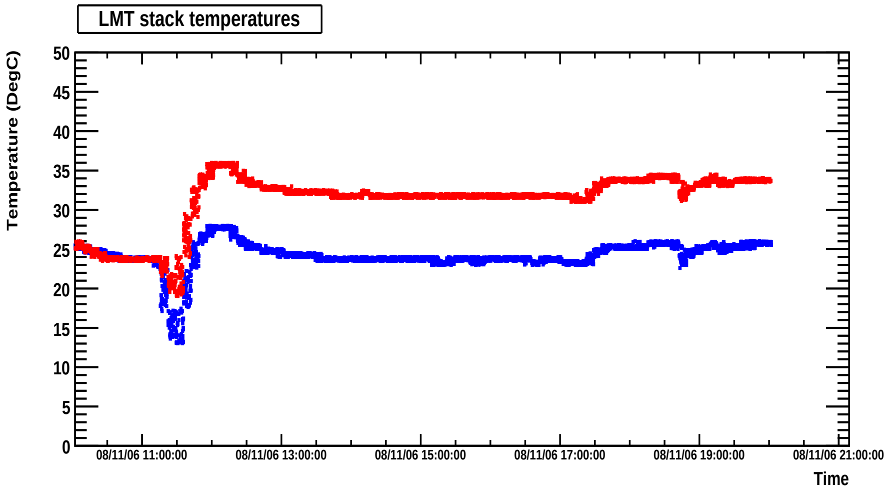


Figure 6.11: Two thermocouples are attached to a stack of LMTs. One at the STFT end where there is no cooling (upper curve), and the other in the middle of the cylinder where there is cooling (lower curve). The temperatures are readout during one full day of testing in November 2006.

Figure 6.11 shows the results. On the x-axis is the time line showing one day of testing from 10am to 8pm. The set-up was configured to allow one octant of all discs to be read out. The upper line (red) shows the temperature of the thermocouple at the STFT end and the lower line (blue) gives the temperature of the cooled LMT thermocouple. Initially there is no cooling and both thermocouples measure the surrounding room temperature environment. In fact there was a mis-calibration factor to consider since the room temperature was actually closer to 20 °C. So the results are all about 5 °C greater and this should be taken into consideration. Next, the cooling was switched on, giving a drop in each temperature readout. All the modules were powered (LV and HV) but there was no data transfer or configuration sent to the module. This gave the sudden rise in temperature for each of the thermocouples. Then follows a plateau where all the modules remained powered on, but were configured and an electrical characterisation performed. Once each disc has been tested, all the modules were configured together and a gain and noise occupancy test carried out. With all the disc octants configured simultaneously, this caused a small rise in the temperature readings, ($\sim$ 3°C) as a result of higher chip currents.

There were two time blocks where the discs were tested simultaneously, one where the heaters on the outer thermal enclosure were switched on and the other when the heaters were switched off. These are shown by the two raised temperature periods between 17:30 and 20:00. From the graph it is clear that the cooling for the LMTs reduces the upper LMT temperature by approximately 8 °C.

A study was performed using a simulation to predict the temperatures of the LMT stack being cooled. From reference [36] the model predicts that there will be a differential temperature of $\sim$ 20°C between the outermost LMT and the cooling pipe. The temperature of our coolant was close to 0 °C and the cooled LMT gives a reading of around 24 °C. If we correct for the mis-calibration of the sensors then these results agree with those determined by the simulation. Since the most central LMT within the group is presumably much hotter, the model predicts a temperature difference of 15 °C between the most inner core of the stack and the outermost LMT.

6.3 Noise and Noise occupancy

In the next sections, the results from the noise and noise occupancy tests will be discussed. At Nikhef and CERN, the analogue and digital tests described in appendix B were performed throughout the assembly process of the endcap. We mark four milestones which are completion of a disc, completion of a cylinder, reception test at CERN, and finally after the installation of the endcap in the cavern.

6.3.1 Input Noise

A “*3Pt-gain*” test was the quickest form of testing the module to see that it was well within the specifications for input noise and channel efficiency. The gain, VT_{50} and offsets for each module as well as a list of all the defective channels can be extracted from the scan. A more precise measurement of the noise can be made by performing a response curve. The response curve is more elaborate but determines the gain by using ten different injection charges as opposed to three charges for the 3Pt gain test.

Figure 6.12 gives a typical example of the response curve of the injected charges and their corresponding VT_{50} points for the 12 chips of module 3A-BL-O1. The gain was calculated using a linear fit with an exponential correction term to the data points. Figure 6.13 shows a plot of the gain distribution for tests taken in the cavern. The data is divided into the four different module groups. Table 6.4 gives the mean and standard deviation of the gain, offset and VT_{50} points of the corresponding data.

Module type	Gain (mV/fC)	Offset (mV)	VT_{50} (mV)
Outers	52.64 ± 2.63	47.70 ± 17.37	153.50 ± 17.99
Middles	53.24 ± 1.59	45.63 ± 15.09	152.30 ± 15.67
Short Middles	55.72 ± 1.41	42.43 ± 13.43	154.02 ± 13.73
Inners	54.67 ± 1.62	43.33 ± 15.14	152.70 ± 14.77

Table 6.4: A summary of the gains, offsets and VT_{50} points for modules installed in the cavern

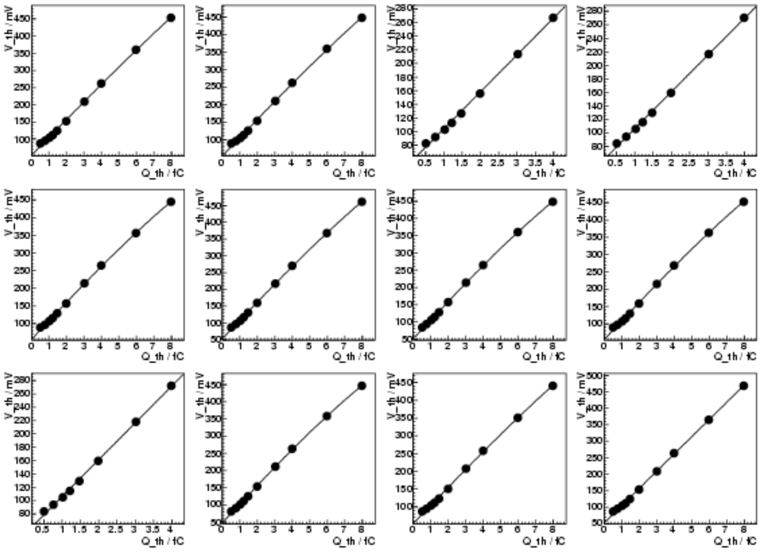


Figure 6.12: The response curve of module 3A-BL-O1 at Nikhef in the disc test box. On the x-axis is the injected charge in fC and on the y-axis it the threshold that gives 50% occupancy.

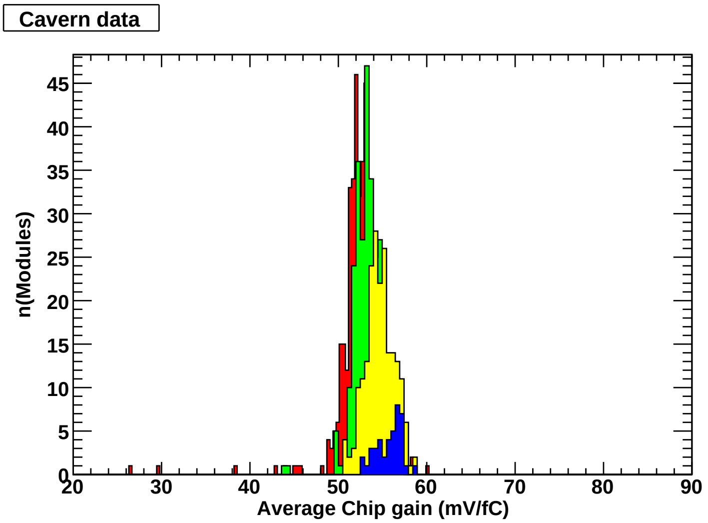


Figure 6.13: The distribution of the gain calculated for each chip of all 988 modules during testing in the cavern. Red (outers), green (middles), yellow (inners) and blue (short-middles).

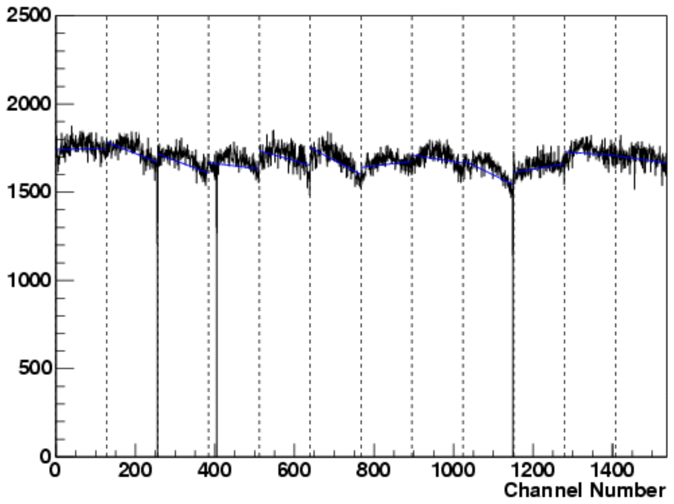
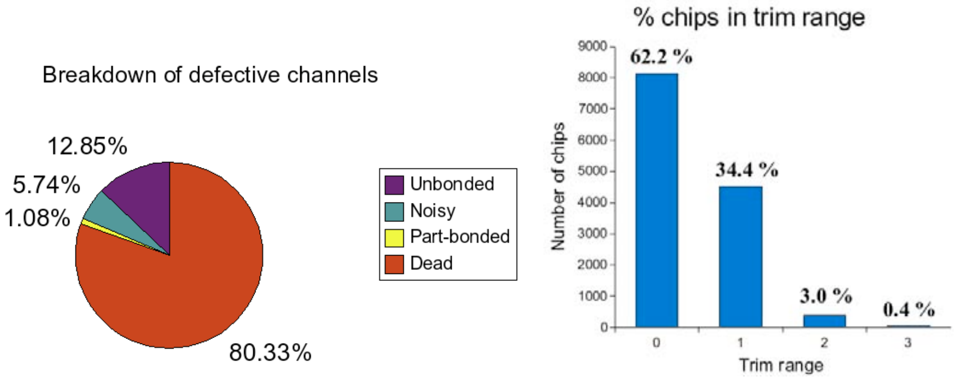


Figure 6.14: The input noise calculated for each of the 1536 channels of module 3A-BL-O1. Here 3 dead channels are present, representing the black vertical lines.

Figure 6.14 shows the input noise to the amplifier for an outer module determined by the response curve scan. The black lines represent *dead* strips in the modules. This means that a strip is not responsive to any charge and will always output a “0”. A strip which is *stuckon* will always output a “1” even if there is no hit. Both of these defects are most likely due to an error in the front-end chip. The specification allows 1% of the strips to be defective. There are several categories for strip defects. A strip is said to be *Noisy* if its value is more than 15% noisier than the average strip on the same chip. This can be caused as a result of a scratch on the aluminium readout strip. A local breakdown can occur, causing an increase in the strip leakage current, consequently leading to a higher noise. Shorts between several strips can also lead to a higher capacitive load input to the amplifier, also leading to an increase in noise. They also reduce the resolution of the detector since the charge will be shared between the strips. A *part-bonded* strip can be spotted when the noise is less than 1100 e. This is usually due to a break in the bond between the two sensors joined together on one side. The capacitance load is reduced, resulting in a reduction in noise for this channel. Similarly, an *unbonded* channel occurs when the noise is less than 800 e. During module manufacture tests, if an unbonded channel was found, it was usually due to a missing bond between the hybrid and the sensor. The module was then sent back for re-bonding.

Figure 6.15a shows the breakdown of channel defects for Endcap-A. During tests, there were three problematic chips. Chip-S3 on 9A-TR-O3 was confirmed *dead* during the tests, causing a loss in 128 channels for that module. Also M0 on 1A-BR-M6 and S1 on 1A-TL-O12 caused scans to fail. Therefore, these chips were by-passed. In the case of M0, both links had to be read out via link one, since reading via the optical link 0 was only allowed if M0 was working. In total 3897 strips were defective for Endcap-A. This gives an overall efficiency of 99.7% of working strips.

To compensate for a variation in response between channels, the modules are trimmed, as described in chapter 4. If a module has not been trimmed properly, then the input noise of the scan will show this, since the variation from channel to channel is noticeable. Most of the modules fall into trim range 0. Figure 6.15b gives an overview of the percentage of modules that are within the possible ranges of 0 - 3.



(a) (b)

Figure 6.15: (a) gives a breakdown of the defective channels, (b) shows the percentage of chips that are in the four different trim ranges.

Depending on the module type, the input noise level will vary accordingly. For inner and short-middle modules that consist of only one sensor one each module side, the length of the module strip is much shorter than an outer or middle module. This results in the noise at the input to the amplifier being lower.

Within the SCT community, it is generally assumed that the temperature dependence of the input noise is approximately 5 ENC/°C. However, more information is now available for endcap modules. At numerous stages during assembly, measurements of input noise and module temperatures have been recorded. There is a spread in the temperatures, allowing the extraction of the noise temperature coefficient. The temperature range is limited, and there is quite some variation in noise from module to module, limiting the precision of this measurement. Figure 6.16 shows the input noise versus temperature measurements for each module type. The data are taken from the various stages of testing both at Nikhef and CERN. It is a profile plot where the input noise data points are averaged for each bin. The results of the fits are included in Table 6.5. The measured noise temperature coefficients for the outers and middles are in agreement with 5 ENC/°C. For the inners and short-middles, the coefficients are less.

Module Type	ENC/°C
OUTERS	5.77 ± 0.27
MIDDLES	4.85± 0.28
INNERS	3.86 ± 0.21
SHORT-MIDDLES	3.72 ± 0.62

Table 6.5: The temperature coefficients extracted from plotting module input noise vs hybrid

For the fits, the errors on the noise measurement were fixed as follows. The input noises were histogrammed using all data sets available, with values from the four main test stages. The rms of the spread was taken as the error. A linear fit was applied to the noise versus temperature data. The resulting slope from the final fit can now be used to adjust the input noises to a certain hybrid temperature. The error estimate yields a $\chi^2/NDF \sim 1$, which gives confidence that the error on the noise is realistic, and the coefficients are precisely

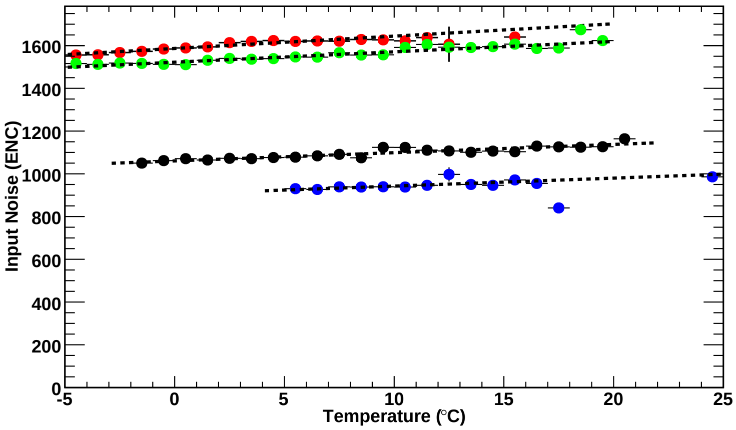


Figure 6.16: Using measured data for the input noise and module temperature, taken during all noise measurements at Nikhef and CERN, a value for the temperature coefficient is extracted. This is performed for each module type. Outers (red), middles (green), inners (black) and short-middles (blue).

determined.

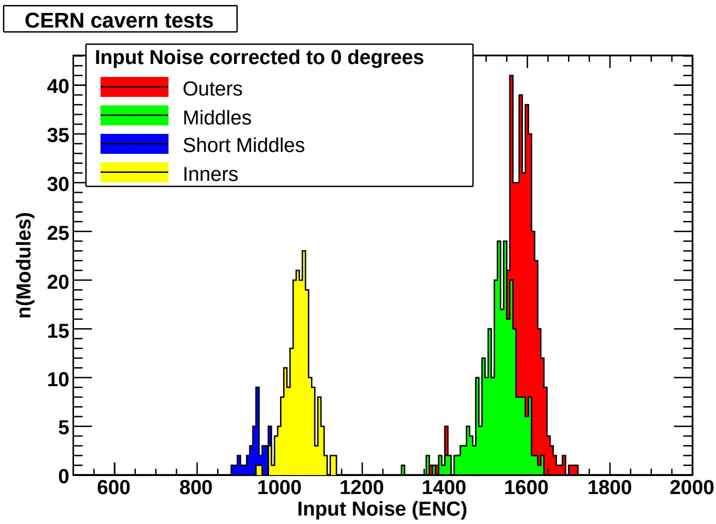


Figure 6.17: The distribution of the input noise during tests in the ATLAS cavern.

Figure 6.17 shows the spread in the input noise for each module group for data taken in the ATLAS cavern. Using the determined coefficients, the data have been normalised to a module temperature of 0°C. Table 6.6 gives a comparison of the mean values and spreads of the input noise for the main stages of testing. From Table 6.6 all values of the input noise are comparable at each stage of testing. There are no signs of module damage over the course of time, including the transportation to CERN and the pit installation.

Test Stage	OUTER	MIDDLE	INNER	SHORT-MIDDLE
Disc completion	1606 ± 51	1527 ± 44	1066 ± 31	911 ± 25
Cylinder completion	1586 ± 52	1519 ± 45	1057 ± 33	908 ± 25
CERN reception	1584 ± 77	1534 ± 62	1055 ± 44	895 ± 38
ATLAS cavern	1608 ± 83	1559 ± 51	1072 ± 32	911 ± 26

Table 6.6: A summary of the mean input noise and spreads during the four main stages of testing (given in ENC). All values have been normalised to a module temperature of 0 °C.

6.3.2 Octant tests and Noise Occupancy results

During the period of testing in SR1, an octant of each disc was connected up to power supplies and the DAQ system so that additional tests could be carried out. The purpose of this test set-up was to run an octant of all discs simultaneously to check for any noise cross-talk between modules. The thermal enclosures at this stage had also been installed. Input noise and noise occupancy tests monitored that the grounding and shielding connections of the enclosures were also functioning correctly. All discs except for disc 9 were connected. (Disc 9 had a leak in one of the cooling connections and therefore had to be left out of the configuration. This was repaired before installation in the cavern.) The TL octant consisted of Outers 1-6, Middles 1-4 and Inners 1-5. Initially input noise and noise occupancy measurements were performed for each disc octant consecutively. Then all the octants were run simultaneously. During the concurrent tests, four heaters of the outer thermal enclosure corresponding to the positions of the octant modules, were cycled on and off to give a heater temperature between 27-30 °C. The results of all tests were compared and analysed both to the octant data set as well as the data taken during initial reception tests at CERN. There was no evidence of module crosstalk or bad grounding and shielding connections.

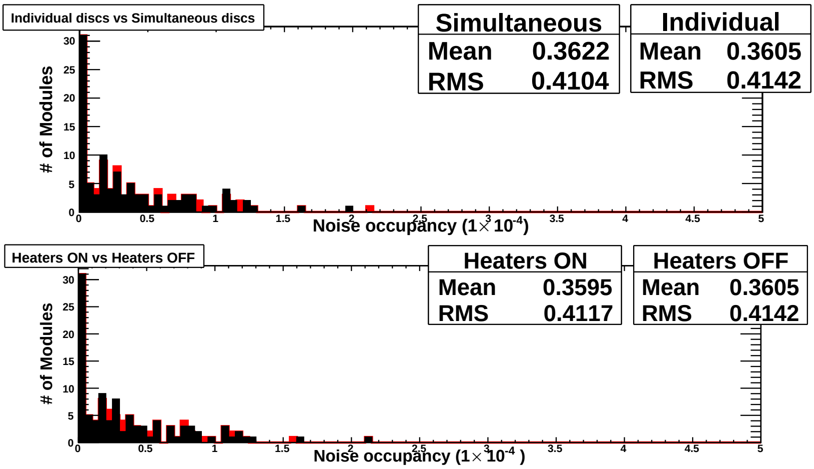


Figure 6.18: Upper plot shows the noise occupancies of individual (red) and concurrent disc testing (black). The lower plot shows the results of all discs run simultaneously for heaters ON (red) and OFF (black).

Figure 6.18 shows the results for the Noise occupancy. The upper plot shows a comparison between the noise occupancy measured on individual disc tests (given in red) and simultaneously run discs (given in black), and the lower plot shows the results when all discs were powered and run together with the heaters switched ON (given in red) and OFF (given in black). The noise occupancy was re-measured once the detector was installed in the ATLAS cavern. The results gave similar values. The specification for noise occupancy is 5×10^{-4}. The results from all occupancy tests show that the Endcap-A modules are well within this criteria.

6.4 Summary and Conclusions

The assembly of Endcap-A, from module production to installation in the ATLAS cavern was achieved working together with engineers, technicians and physicists. Nikhef produced 100 inner modules which were mounted onto endcap discs. The remainder came from participating institutes within ATLAS. Endcap-A has been extensively tested both at Nikhef during macro assembly and upon reception and integration at CERN. The endcap was successively installed, together with the TRT in its final position within the ATLAS cavern in May 2007.

The optical links used to send commands and read the data from the modules have been analysed. More than 98.7% of the links are fully functional. One *p-i-n* diode was unresponsive and 26 *VCSEL*s were either declared *dead* or too problematic to read out the data. The redundancy scheme allowed the recovery of these links. In the case of the *p-i-n* diode that was *dead*, its module, received clock and command signals from its neighbour. The bad RX links were read out via the other working link of the module.

A series of I-V scans have been performed on all modules. All modules ramp up to 350 V without junction breakdown. CiS detector modules, with their non-field plate geometry are more susceptible to micro-discharge early on in the scan. Several modules required training in a moist environment before enabling a full scan to 350 V in a dry atmosphere.

Evaporative cooling using C_3F_8 is used to keep the sensors cold as well as to remove heat dissipated by the chips. The quality of the connections of cooling blocks to pipes proved excellent, ensuring a minimal spread in module temperatures. One-sided cooling to the LMTs also effectively reduce their temperature caused as a result of the currents induced in the cables. Successful integration of the inner and thermal enclosures act as a barrier between the SCT and TRT sub-systems. Nitrogen will be used to keep the SCT detector dew-point low enough for a coolant temperature set at -25°C. The thermal enclosures have been thoroughly tested and a leak rate of 85 litres/hr achieved. These are well within the specifications laid out by ATLAS.

The input noise to the amplifier of each module channel has been extensively tested from module production through to the final ATLAS installation. There were no significant changes in the noise even after all levels of transportation and integration steps. The grounding and shielding of the thermal enclosures as well as the connection to the TRT have proved highly efficient. Over 99.7% of the module channels are fully working, which is well within the specification of 1% allowed defective channels. Both sides of all 988 modules are able to be readout, with the exception of one dead and two problematic chips.

A study of the input noise versus hybrid temperature gives results of temperature coefficients for each module type. The general assumption of 5 ENC/K is true for modules of outer type, but for the others, their temperature coefficients are lower. The general trend that outer coefficients are larger than middles and inners is apparent.

Finally, the noise occupancy has been tested during octant tests in SR1 and the ATLAS cavern. The modules were all found to be less than the limit of 5×10^{-4} by a factor of ten.

CHAPTER 7

DETECTOR NOISE

*"It doesn't matter how beautiful your theory is, it doesn't matter how smart you are.
If it doesn't agree with experiment, it's wrong."*

Richard Feynman

Contents

7.1 Noise Mechanisms

The following sections give an overview of noise sources for the front-end electronics and the sensor. For the purpose of this work, seven noise contributions will be considered based on the series and parallel noise components of an SCT detector module. Figure 7.1 shows a schematic of a detector module. The current and voltage induced noise sources which correspond to this schematic are given in Table 7.1.

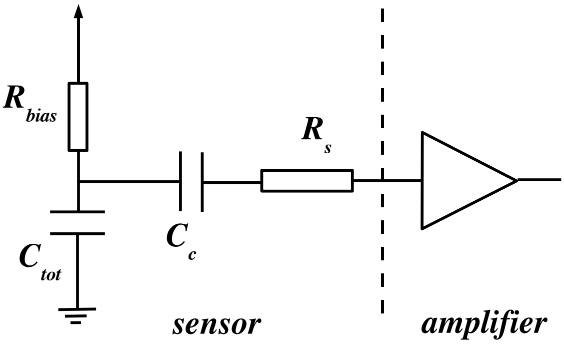


Figure 7.1: Schematic view of an SCT detector module showing the noise sources. R_{bias} denotes the bias resistor, C_{tot} is the total capacitance of a strip, C_c is the coupling capacitance and R_s is the strip resistance.

source	name	component	symbol	related parameter
voltage	BJT base-spread resistance	amplifier	e_{bb}	R_{bb}
voltage	BJT collector current	amplifier	e_c	I_c
voltage	sensor strip resistance	sensor	e_s	R_s
current	BJT base current	amplifier	i_b	I_b
current	feedback resistance	amplifier	i_f	R_f
current	strip leakage current	sensor	i_l	I_l
current	strip bias resistance	sensor	i_{bias}	R_{bias}

Table 7.1: Overview of noise sources in an SCT detector module considered throughout this work.

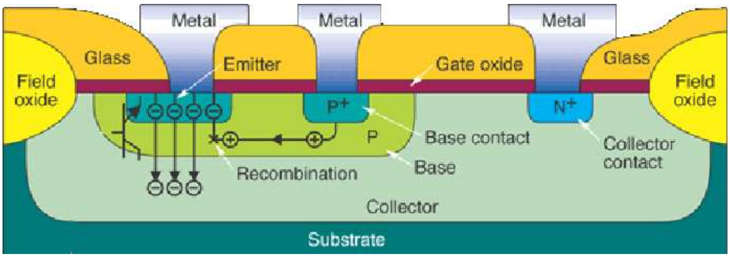


Figure 7.2: Cross section and principle of operation of a bipolar transistor in CMOS technology.

7.1.1 Front-end electronics

The amplification process dominates the noise performance and for this reason is crucial to the overall operation of the detector. For simplification, the noise of the amplifier system can be expressed as an ideal noiseless amplifier plus series and parallel noise sources. For the purposes of this work four sources in the amplifier will be considered. Figure 7.2 represents the basic layout of a bi-polar junction transistor (BJT), the basis of the ABCD chip. It consists of two back to back n-p junctions, which share a thin, common region. Contacts are made to all three regions, the two outer regions called the emitter and collector and the middle region called the base. Its operation involves both types of mobile carriers, electrons and holes, hence the name *bi-polar*.

In the forward active mode of operation, obtained by forward biasing the base-emitter junction and reverse biasing the base collector junction, electrons diffuse from the emitter into the base and holes diffuse from the base into the emitter. The electric field sweeps the minority carriers at the base-collector depletion region, through the depletion layer. The electrons contribute to the collector current and their random arrival time at the collector base junction, results in a series of random pulses, conveying shot noise behaviour. It is this current that determines the operation point of the amplifier and has an important effect on the output voltage.

The model commonly used for circuit analysis is the hybrid-π model [73]. This model describes the effective output current noise caused by the collector current i_c as an effective input voltage noise source:

$$\langle {e_c}^2 \rangle = \frac{\langle {i_c}^2 \rangle}{{g_m}^2} \quad \text{and} \quad g_m = \frac{q_e I_c}{k T_c} \tag{7.1}$$

where g_m is the trans-inductance of the transistor, k is Boltzmann's constant and T_c is the absolute temperature of the silicon chip. By substituting in the following equation for a current noise source expressed per unit frequency:

$$\langle {i_c}^2 \rangle = \langle 2 q_e I_c \rangle \tag{7.2}$$

where q_e is the electron charge, I_c is the DC collector current, the formula for the I_c shot noise becomes:

$$\langle {e_c}^2 \rangle = \frac{2k^2 {T_c}^2}{q_e I_c}. \tag{7.3}$$

The second source of shot noise is that due to the base current. It can be related to the collector current by the short circuit current gain, β, of the transistor:

$$\langle {i_b}^2 \rangle = \frac{2 q_e I_c}{\beta}, \tag{7.4}$$

where $I_b = \frac{I_c}{\beta}$, the DC base current, and can be expressed as:

$$\beta = \beta_0 \frac{T_{c,0}}{T_c} \tag{7.5}$$

where β_0 is the current gain at the reference chip temperature $T_{c,0}$. In the hybrid-π model the fluctuations of the emitter current are not correlated with the fluctuations of the collector current, therefore the two shot noise sources are not directly related. This is not the case for the ABCD design, however the differences between the simple noise model and the correlated model are small and neglected here [67].

In addition to the current noise sources I_c and I_b, one also has to consider the thermal noise from the parasitic contacts and the bulk resistance. The most important parameter is the base spread resistance, R_{bb} with its voltage noise source per unit frequency:

$$\langle {e_{bb}}^2 \rangle = 4kTR_{bb} \tag{7.6}$$

R_{bb} is temperature dependant and can be expressed in terms of its value R_0 at a reference chip temperature $T_{c,0}$ for some other temperature T_c by:

$$R_{bb} = R_0 \frac{{T_{c,0}}^{-1.5}}{{T_c}^{-1.5}} \tag{7.7}$$

R_{bb} is determined by the base doping and the transistor geometry. The base of the BJT is very thin, giving high resistance. It is the most dominant parameter since it appears at the input terminal, giving the largest contribution to the noise. Its value also greatly depends on acoustic lattice scattering. This is scattering of the free carriers by interaction with lattice atoms as they move in acoustic vibrational modes due to thermal energy. The temperature dependence of the base material has a $T^{-1.5}$ dependency.

The final amplifier noise source to be taken into account is the thermal noise generated by the influence of the feedback resistor R_f:

$$\langle {i_f}^2 \rangle = \frac{4kT}{R_f}. \tag{7.8}$$

7.1.2 Sensor

There are three sources in the silicon sensor that contribute to the overall detector noise.

1. The leakage current is due to the generation current which is proportional to the number of intrinsic charge carriers in the depleted region. It is related to the temperature and bias voltage of the sensor by Equation 7.9:

$$I_l = \begin{cases} I_0 \cdot \dfrac{T_s^2}{T_{s,0}^2} \cdot e^{\frac{1.2q_e(T_s - T_{s,0})}{2kT_sT_{s,0}}} \cdot \sqrt{\dfrac{V_{bias}}{V_{dep}}} & V_{bias} \leq V_{dep} \\ I_0 \cdot \dfrac{T_s^2}{T_{s,0}^2} \cdot e^{\frac{1.2q_e(T_s - T_{s,0})}{2kT_sT_{s,0}}} & V_{bias} > V_{dep} \end{cases} \tag{7.9}$$

   where I_0 is the leakage current at the sensor temperature $T_{s,0}$, q_e is the electron charge and k is Boltzmann's constant. The factor of 1.2 in the equation is the band gap energy in silicon.

   This leakage current gives rise to a noise current source $\langle {i_l}^2 \rangle = 2q_eI_l$. Un-irradiated sensors have very low leakage current, but radiation damage causes it to rise so it can give an appreciable noise level at the end of life.

2. The p^+ implant strips are connected to the bias rail via resistors R_{bias} in the detector. They give a current noise per unit frequency:

$$\langle {i_{bias}}^2 \rangle = \frac{4kT_s}{R_{bias}} \tag{7.10}$$

3. The strip resistance is a voltage noise source, generated by the resistance of the aluminium traces that are layered on top of the silicon read-out strips. The voltage noise per unit frequency is given by:

$$\langle {e_s}^2 \rangle = \frac{4kT_s}{R_s} \tag{7.11}$$

7.1.3 Capacitances

The total input capacitance seen by the amplifier has a large impact on the absolute noise output. This is a very important parameter, affecting both noise and crosstalk. There are five components considered in this work which contribute to the total capacitance of the detector. Both the strip to strip capacitance and the strip to back-plane capacitance are substantial factors in the overall capacitance of the silicon sensor. The strip to strip capacitance is the capacitance between the silicon strip of the sensor and its neighbouring strips. C_{sb} is the capacitance between the strip and the sensor back-plane. Lastly, there are the capacitances due to the front-end electronics. There is the capacitance load due to the feedback capacitor, C_f. There is also the capacitance C_a due to the capacitor located at the input to the charge sensitive preamplifier. The stray input capacitance C_{stray} must also be considered. Due to the large bonds and pitch adapters on the detector C_{stray} is expected to be approximately 1 pF (1.5 pF) for a SCT barrel (endcap) module. There is also the coupling capacitance which blocks the sensor bias voltage from the amplifier input. It has a very large value (25 pF) and is therefore considered negligible when adding capacitors in parallel.

7.1.3.1 Strip to back-plane capacitance

This strip to back-plane capacitance is proportional to the area related to one strip and inversely proportional to the detector thickness. C_{sb} increases with the applied bias voltage until it reaches the depletion voltage, at which point the value is stable. Equation 7.12 gives the bias dependence of C_{sb}:

$$C_{sb} = \begin{cases} C_0 \cdot \sqrt{\frac{V_{dep}}{V_{bias}}} & V_{bias} \leq V_{dep} \\ C_0 & V_{bias} > V_{dep} \end{cases} \tag{7.12}$$

where C_0 is the fully depleted strip-to-back-plane capacitance, given by:

$$C_0 = \frac{\epsilon_0 \epsilon_r A}{d} \tag{7.13}$$

where ϵ_0 is the permittivity of free space, ϵ_r is the dielectric constant of silicon, A is the area of the capacitor (pitch × strip length × number of strips) and d is the distance between the capacitor plates. Substituting the known values for a W12 wafer, this equation gives 35.91 pF/cm^2 for the fully depleted strip to back-plane capacitance. NIKHEF, MPI and Lancaster university have measured this parameter and the results agree with the value obtained from the mathematical description of C_{sb}.

In Lancaster, the total strip to back plane capacitance between the front and back-planes for several wafer types were measured (W12, W21 and W22 wafers.) The capacitance per unit area ideally should be the same for all three types. This is true with an accuracy of about 2%. Column "C_{sbtot}" gives the average measured or estimated values of the strip to back-plane capacitance added over all strips. The strip capacitance C_{sb} is then obtained by dividing the total capacitance (either measured or estimated) by the number of strips.

At NIKHEF and MPI, the strip to back plane capacitances were estimated using numerical predictions from TOSCA to calculate the dielectric constant for the silicon material used in the SCT sensors. With this constant an estimate for C_{sb} was deduced. Since each detector wafer has a different strip pitch, the equation deduces a C_{sb} value for each wafer. Table 7.2 summarises all the results.

Table 7.2: Summary of strip to back-plane measurements C_{sb} measurements at 150V, taken at Lancaster, MPI and NIKHEF for different wafers (stable detectors). Wafers W31 and W32 have estimates extrapolated from Lancaster's measurements for C_{sb}. The strip to back-plane capacitances were calculated from either the measured or estimated capacitance, divided by the total number of strips.

LANCASTER							MPI/NIKHEF
wafer	length (cm)	pitch (μm)	Area (cm^2)	C_{sbtot} (pF)	C_{sbtot}/A (pF/cm^2)	C_{sb}/cm (pF/cm)	C_{sb}/cm (pF/cm)
W12	5.91	63	28.60	1062	37.14	0.23	0.21
W21	6.31	76.4	37.02	1338	36.04	0.28	0.25
W22	5.25	88.8	35.80	1269	35.35	0.29	0.29
W31	6.36	76.0	37.12	1345[a]	–	0.28	0.25
W32	5.56	86.0	36.72	1331[a]	–	0.29	0.28

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[a] These capacitance values have been estimated using the results of the measured W12, W21 and W22 wafers. A capacitance per unit area of $\approx$ 36 pF/cm was taken and this value multiplied by the area in column 4 to give C_{sbtot}.

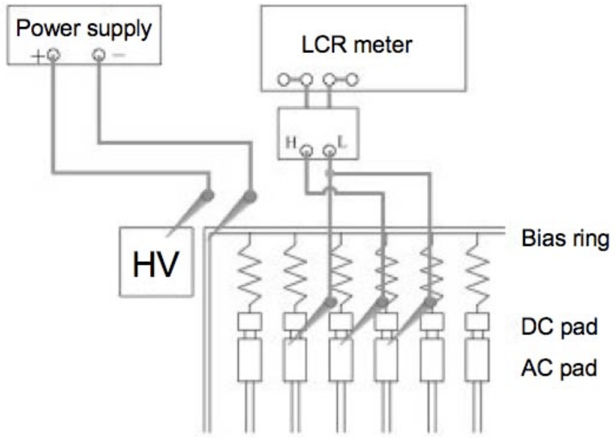


Figure 7.3: Schematic showing the capacitance measurement setup for a central strip biased and its neighbouring strips grounded. The total capacitance is measured between the AC pad and the electrode.

7.1.3.2 Total strip capacitance

From reference [65], the total-strip capacitance can be estimated as:

$$C_{tot} = C_{sb} + 2C_{ss} \tag{7.14}$$

where C_{ss} is the strip to strip capacitance and C_{sb} the strip-to-backplane capacitance. Throughout this work and the references for the data taken at the Max Planck Institute (MPI) and NIKHEF, the total-strip capacitance measurements are denoted as C_{tot}. References presenting data given by Lancaster, given by Equation 7.14 are denoted C_{is}.

The standard quality and assurance procedure for taking a C_{tot} measurement is to install a sensor in a frame and use three probe needles to measure a capacitance between a strip and its two nearest neighbours as a function of bias voltage. The central strip is biased at a voltage between 0-150 V and the neighbouring strips are grounded. The total capacitance between the AC pad and the electrode is measured. The value of C_{tot} at 150 V is taken to be the total-strip capacitance for a given wafer and is denoted as C_{150}.

Figure 7.3 shows the capacitance set-up. The results of an investigation into C_{tot} by Alex Chilingarov et al. [23] at Lancaster University, give a better understanding of the actual behaviour of the inter-strip capacitance. They show that after initial application of the bias voltage, C_{tot} decreases with time. It was also noticed that the time required for the capacitance values to reach their stable values (t_{stab}), strongly increases with the decrease in the ambient humidity. From data measured at Lancaster a difference of up to 19% was measured between the starting and nominal C_{tot} values for five sensors [21]. Figure 7.4 shows the strong dependence of the stabilisation of C_{tot} as a function of time.

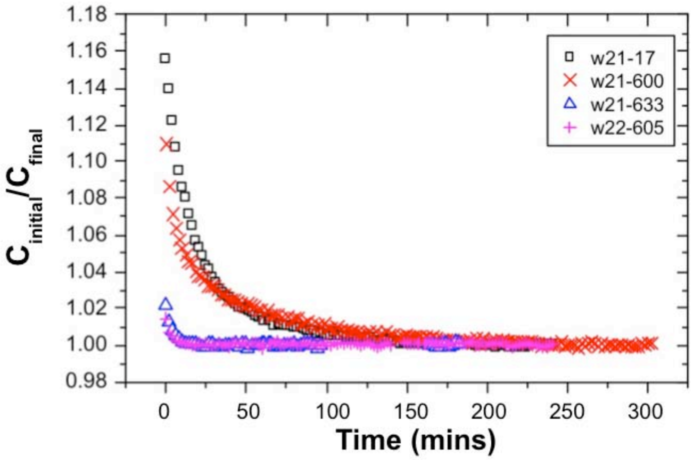


Figure 7.4: The normalised total-strip capacitance as a function of time (mins) after 150 V bias application for four different sensors. This data was taken at Lancaster [21].

For determining C_{tot}, two measurement methods at Lancaster were investigated: measurements for charged surface sensors (fresh sensors) and measurement for depleted charge sensors (stable sensors).

Stable sensors

Using W12, W21 and W22 wafers, C_{tot} measurements were taken at 150 V whilst waiting a long time for the detector surface to be uncharged corresponding to the stable state of the detector module. Estimations for wafers W31 and W32 were calculated. This was achieved since C_{tot} is linearly proportional to the inverse of the detector pitch [65]. These capacitance values are described as being nominal.

MPI and NIKHEF also measured the total-strip capacitance of each SCT wafer type. NIKHEF measured the C_{tot} for a W12 wafer and MPI provided the data for the remaining wafers. The set-up measured the capacitance for stable wafers, when two of the immediate neighbours were grounded. Measuring with only one nearest neighbour on either side will yield a value smaller than if the measurement had been taken with nine or more neighbours. Since there are 768 strips on one side of a detector module, the actual values of C_{tot} have not been measured. Table 7.3 gives a summary of the capacitance findings for *'stable'*

		MPI/NIKHEF	LANCASTER
wafer	pitch (μm)	C_{150}/length (pF/cm)	C_{150}/length (pF/cm)
W12	63.0	0.79	0.83
W21	76.4	0.73	0.74
W22	88.8	0.67	0.65
W31	76.0	0.75	0.74
W32	86.0	0.69	0.71

Table 7.3: Summary of MPI and NIKHEF measurements of C_{150}, the total strip capacitance at 150 V.

detector modules for all institutes. From reference [65], a simulation of C_{tot} was performed using TOSCA for a barrel wafer of pitch 80 μm. Two simulations were investigated, one simulating the total-strip capacitance where only two neighbouring strips were grounded, and another where nine of the neighbouring strips were grounded. The latter set-up being more realistic for that of the SCT module where 768 strips are bonded on each detector side. For two nearest neighbours, C_{tot} = 1.031 pF/cm and for nine grounded strips C_{tot} = 1.061 pF/cm. The capacitance measurements performed at each institute under estimate the real capacitance when all strips of a module are grounded.

Fresh sensors

The second method for measuring C_{tot} was by measuring its value at different bias voltages, whilst being biased for only a short period of time in a dry environment. Short enough for the detector surface to remain charged. These are referred to as "*fresh*" detectors. For wafer types – W12, W21 and W22 – the total-strip capacitance was measured as a function of bias voltage. Figure 7.5 shows the results for these wafers. There are four distinct curves each

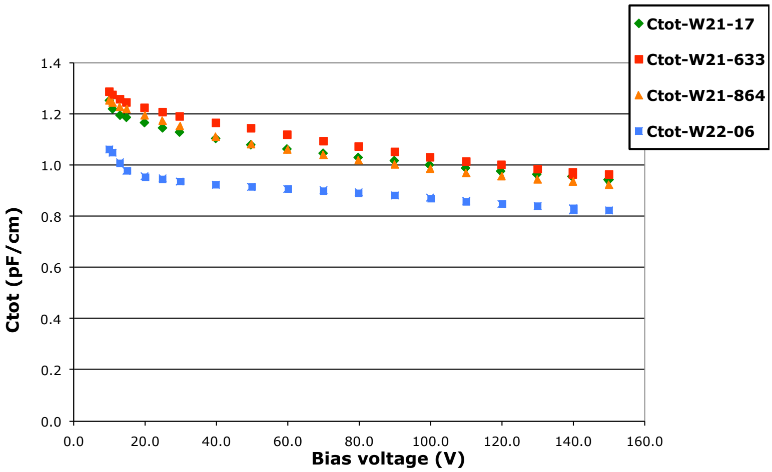


Figure 7.5: C_{tot} measurements for four different wafer types as a function of bias voltage [22].

FRESH detectors		
wafer	pitch (μm)	C_{150}/length (pF/cm)
W21-17	76.4	0.94
W22-633	88.8	0.96
W22-864	88.8	0.92
W22-06	88.8	0.82

Table 7.4: Capacitance values measured by Lancaster, of fresh detectors, biased only for a short time.

representing a different sensor. The values found for the fresh detectors compared with those in Table 7.3 are considerably higher than detectors biased for a longer period. The results reflect the earlier statement that the initial C_{tot} measurement is much higher than if one had biased the detector for a longer time period. Table 7.4 summarises the results of the total-strip capacitance measurements taken at 150 V (C_{150}) at Lancaster.

7.1.3.3 Capacitance conclusions

The measurements for stable detectors given in Tables 7.2 and 7.3 from all institutes, for the two capacitance terms, C_{sb} and C_{150} are very comparable and in agreement with one another. It is useful to note that the total-strip capacitance of the inners (W12 wafers) is higher than that of the outer and middle wafers. This is as a result of the different field plate geometries of the wafers, as explained previously. The comparable results give a good reassurance that when the modules are biased for a long time, a good approximation of C_{150} for each detector type can be established using these values. The values measured for the fresh detectors at Lancaster were considerably higher by approximately 15$\%$ than those taken under more stable conditions.

The total-strip capacitance is extremely important for the optimisation of the operating conditions of the SCT detector. It has been shown that after initial application of the bias voltage, C_{tot} decreases with time. It was also noticed that the time required for the capacitance values to reach their stable values, strongly increases with the decrease in the ambient humidity. This total-strip capacitance effect explains previous observations that after bias application the noise decreases with time. At a temperature of $-10°$C, close to SCT operation, t_{stab} ranges from $\sim$ 1 day to $\sim$ half year, depending on the relative humidity.

During ATLAS running of the SCT, it will be necessary to switch off the bias voltage, due to detector repairs or for shutdown periods. A study performed by A.Chilingarov et al. showed that only a slight increase in C_{tot} was detected after unbiasing the detector for 24 hours, after an initial bias application of 150 V was applied for $\sim$6.3 days. An increase of 0.6$\%$ in C_{tot} was measured which was found to disappear in less than 2 hours after reapplication of the bias [21].

It is clear that careful optimisation of the detector operation will be needed. Under very dry conditions, it will require several months for the detector to reach a stable state. The most efficient method would be to bias the detector at room temperature, before starting to flush with nitrogen. The stabilisation time of C_{tot} would only be of the order of a few hours, long before the SCT tracker volume is cooled and dried to its ATLAS operational values. However, this is not feasible from an operational point of view.

7.2 Noise model

Noise can be quantified in terms of the equivalent noise charge (ENC). It is the value of the charge that needs to be delivered to the pre-amplifier input to produce the same output as the noise. It is expressed in electrons. Equation 7.15 gives the expression for the ENC.

$$ENC = \frac{e^3}{36q_e}\sqrt{\frac{3C^2\langle e_n^2\rangle}{T_p} + \frac{5T_p\langle i_n^2\rangle}{3}} \qquad \text{(electrons)} \tag{7.15}$$

where e is Napier's constant, q_e is the electron charge, e_n is the total voltage noise, T_p is the peaking time and i_n is the total current noise. This formula results from considering separately the effect of the amplifier-shaper on the signal and on the noise, taking the ratio to obtain the SNR, and setting this equal to one to obtain the ENC.

If all the previously derived current and voltage sources are substituted into the above equation, then the expression for the noise in electrons (ENC) is:

$$\begin{aligned} ENC &= \frac{e^3}{36q_e}\left\{\frac{3}{T_p}\left(C_{tot} + C_{stray} + C_a + C_f\right)^2\left(4kT_cR_{bb} + \frac{2k^2T_c^2}{q_eI_c} + 4kT_sR_s\right)\right. \\ &\left. +\frac{5T_p}{3}\left(\frac{2q_eI_c}{\beta} + \frac{4kT_c}{R_f} + 2q_eI_l + \frac{4kT_s}{R_{bias}}\right)\right\}^{\frac{1}{2}} \end{aligned} \tag{7.16}$$

where C_{tot} is the sum of C_{sb} and $2\times C_{ss}$, shown earlier in Figure 3.12 of chapter 3. T_c and T_s are the chip and sensor temperatures, R_{bb} is the base-spread resistance at the chip temperature T_c and β is the current gain at the chip temperature T_c. Recalling from section 7.1.3, C_{sb} and C_{tot} are dependant on the bias voltage parameter V_{bias}.

7.2.1 Simulation of noise contributions

This section shows the results of a simulation based on the previously described noise model. As stated previously, both CiS and Hamamatsu Photonics, are sensor manufacturers. The differences in the module elements are defined in the simulation program to incorporate the two different sensor designs. The simulation provides a breakdown of the total noise contributions of a detector module for each detector type. This allows us to see which parameters are important in dominating the overall noise of the detector. The simulation also evaluates how the noise behaves as a function of the hybrid temperature. The results will be presented in the following sections. This study is an extension of the work performed by Simon Peeters. In his thesis [65] a simulation of the individual noise contributions was made using the above described model. In this work more data has been acquired and a more accurate measurement is presented.

7.2.1.1 Noise model parameters

The noise model has been implemented in a ROOT C++ file. The parameters of the model which are independent of module type, were stored in this file. Table 7.5 gives these parameters. Other parameters vary from module type to module type, Table 7.6 gives these. Two manufacturers -CiS and Hamamatsu Photonics- produced the wafers resulting in two different sets of parameters. Hamamatsu sensors are biased via poly-silicon resistors while CiS sensors use implanted meander resistors. The initial depletion voltage also varies. Hamamatsu sensors require a lower voltage than CiS sensors to fully deplete them. Finally Hamamatsu strips have a lower resistance than CiS ones. The average strip lengths, depletion

Component	Name	Param	Value
AMPLIFIER	current gain	β_0	235 ± 66
	amplifier input capacitance (pF)	C_a	1.00 ± 0.1
	feedback capacitance (pF)	C_f	0.17 ± 0.002
	collector current (μA)	I_c	220
	base-spread resistance (Ω)	R_0	180 ± 7
	feedback resistance (kΩ)	R_f	77 ± 1
	peaking time (ns)	T_p	20 ± 0.5
	chip temperature ($^\circ$C)	T_c	$\sim T_{hyb}$ + 5
	reference temperature chip (K)	$T_{c,0}$	300
SENSOR	stray capacitance (pF)	C_{str}	1.5 ± 0.2
	sensor temperature ($^\circ$C)	T_s	T_{hyb} - 15
	reference temperature sensor (K)	$T_{s,0}$	300

Table 7.5: Summary of the parameters needed for the noise calculation. The values are for an ATLAS SCT detector module. The errors stated are mostly estimates.

Table 7.6: Sensor parameters dependent on manufacturer or module type.

Manufacturer	-	Hamamatsu	Hamamatsu	CiS
Property	Param	Outer	Middle	Inner
Bias resistance (MΩ)	R_{bias}	1.49 ± 0.16	1.49 ± 0.16	0.72 ± 0.07
Strip resistance (Ω/cm)	R_s	8.90 ± 0.09	8.90 ± 0.09	13.8± 0.01
Dep. Voltage (V)	V	64.8	64.8	84.5
Strip length (cm)	l	W31: 6.55 W32: 5.75	W21: 6.51 W22: 5.44	W12: 6.11
Strip to back-plane (pF/cm)	C_{sb}	W31: 0.27 ± 0.01 W32: 0.29 ± 0.01	W21: 0.27 ± 0.02 W22: 0.2 ± 0	W12: 0.22 ± 0.01

voltages and bias and strip resistances are taken from reference [6]. The strip to back plane values are the average of the measurements made by MPI, NIKHEF and Lancaster which were discussed earlier.

7.2.1.2 Main parameter uncertainties

Errors for both the amplifier and sensor parameters must be considered. In the case of the bipolar junction transistor, parameters have a relatively large spread which is typical for most bipolar technologies. The parameters are not accessible by being measured directly which makes the errors somewhat larger. In the case of the base spread resistance, reference [55] gives an accurate measurement of it at room temperature. Its value is 180 Ω with an error of $\sim \pm 7$ Ω.

The current gain, β was the parameter with the largest uncertainty. Its value is between 120 and 350 for un-irradiated chips lowering to around 40 after irradiation [56]. Assuming that the value of β is equally probable along this range for each chip, the actual error is assumed to be the spread divided by $\sqrt{12}$. This gives an error of $\beta = 235 \pm 66$.

The input capacitance C_a is rather stable and its value is expected to be better than 5% giving 2 ± 0.1 pF [28] The peaking time is taken to be 20 ns with an error of 0.5 ns based on reference [37]. The values for the resistors and capacitors in the chip are precisely known. Hence, we take the standard deviation for each batch of a particular parameter and we obtain R_f = 77$\pm$1 kΩ, C_f = 0.170 ± 0.002 pF.

The errors on the sensor parameters, were determined from references [65] and [6]. The bias resistors, the SCT specification was set at 1.25 ± 0.75 MΩ. However, measurements were taken for a selection of modules using Hamamatsu wafers and the spread of the group was determined. Table 7.6 shows the results. The standard deviation was measured and found to be $\sim$ 11%. The same error is assumed for the CiS modules. Table 7.6 also shows the average values found for the sensor strip resistance. Here, also a sample of Hamamatsu sensors were measured. The specifications are set at $R_s < 15$ Ω/cm, and for each module manufacturer the average was less than this value. An error of 10% is estimated.

All of these errors are used in the simulation to calculate an error for each noise contributor. These are then added in quadrature in the final calculations of the overall error on the noise.

7.2.1.3 Estimation of the sensor temperature

The temperature of the hybrid for each module is monitored. For end-cap modules there is a sensor located on the hybrid for this purpose. This temperature is recorded by the software during a test and is therefore later accessible from the summary text file. This temperature is referred to as T_{hyb}. The noise model requires the chip and sensor temperatures, which differ from T_{hyb}, but by a reasonably constant amount. The differences have been estimated from a thermal photograph taken at Liverpool for Disk 9C, Figure 7.6 [53]. It shows that the module sensors are much colder than the ASICs with the hybrid in-between. From the colour scale, the sensors are about 15 °C cooler than the hybrid and the chip is about 5 °C hotter. We therefore take T_c = T_{hyb} + 5 °C and $T_s = T_{hyb} - 15$°C.

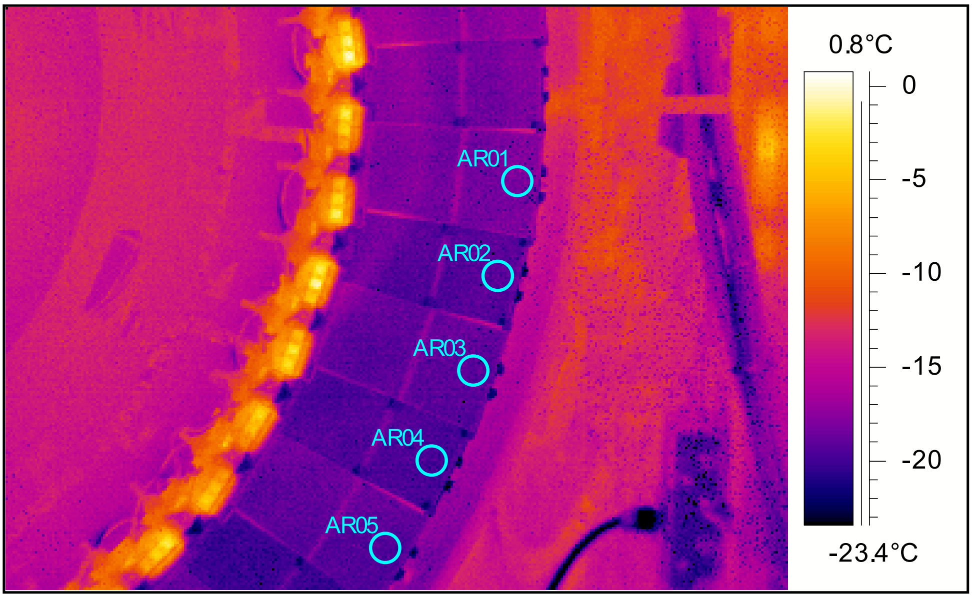


Figure 7.6: A thermal photograph taken of BR O1-O5 for Disk 9C. The silicon wafers are much cooler than the readout ASICS. The circles denote the module present at that position. Closest to the top is Outer 1, leading to Outer 5 at the bottom.

7.2.2 Determining noise contributions

Using Equation 7.16 the simulation calculates the individual current and voltage noise sources for each detector type. In the simulation each detector type is biased at a voltage of 150 V and has a hybrid temperature of 15 °C. The average values of C_{sb} and C_{150} for a stable detector measured at the previous mentioned institutes will serve as input to the noise model. A simulation has been implemented to calculate the individual contributions which make up the overall noise.

The equations below show the way in which the different contributions were determined in the simulation.

$$ENC_b = \frac{e^3}{36q_e}\sqrt{\frac{5T_p}{3}\left(\frac{2q_eI_c}{\beta}\right)}$$

$$ENC_f = \frac{e^3}{36q_e}\sqrt{\frac{5T_p}{3}\left(\frac{4kT_c}{R_f}\right)}$$

$$ENC_l = \frac{e^3}{36q_e}\sqrt{\frac{5T_p}{3}\left(2q_eI_l\right)}$$

$$ENC_{bias} = \frac{e^3}{36q_e}\sqrt{\frac{5T_p}{3}\left(\frac{4kT_s}{R_b}\right)}$$

$$ENC_{bb} = \frac{e^3}{36q_e}\sqrt{\frac{3}{T_p}\left(C\right)^2\left(4kT_cR_{bb}\right)}$$

$$ENC_c = \frac{e^3}{36q_e}\sqrt{\frac{3}{T_p}\left(C\right)^2\left(\frac{2k^2T_c^2}{q_eI_c}\right)}$$

$$ENC_s = \frac{e^3}{36q_e}\sqrt{\frac{3}{T_p}\left(C\right)^2\left(4kT_sR_s\right)}$$

where $C = 2C_{ss} + C_{sb} + C_{str} + C_a + C_f$. Each contribution has a dominating parameter which is defined later on in Table 7.7.

7.2.3 Combining errors

For each parameter given in Table 7.5, there is an associated error. These errors are described in 7.2.1.2, where it states that for each noise term there is a dominating parameter with a specific error. Consequently, each noise contribution term has an error too, based on this parameter error. The noise error for each contributing term is computed in the following way. By taking the mean difference between the two noise calculations for this parameter, X, determined by substituting $(X + \sigma_x)$ and $(X - \sigma_x)$, into the equations specified in sub-section 7.2.2. Where σ_x is the error associated to the parameter.

To be able to quantify the total error on the noise, we must combine several independent error sources from the same measurement. This is achieved by using error propagation. Both current and voltage noise source errors define the total error. The errors in the the current sources are just as likely to (partially) cancel the errors in the voltage sources, as they are to add to it. In order to preserve the probability of both errors, we add in quadrature. For each error source there are strong correlations between the individual error components. This is taken into consideration by adding the correlated terms together before squaring them. Equations 7.17-7.19 show the formulae used to calculate the overall noise error, denoted by σ_{ENC}. *ENC* denotes the overall noise of the detector.

$$\sigma_{\langle i_n{}^2\rangle} = \sqrt{\sigma^2_{R_{bb}} + (\sigma_{I_c} + \sigma_{R_s})^2} \tag{7.17}$$

$$\sigma_{\langle e_n{}^2\rangle} = \sqrt{\sigma^2_{R_b} + \sigma^2_{R_f} + (\sigma_{I_l} + \sigma_{R_{bias}})^2} \tag{7.18}$$

$$\sigma_{ENC^2} = \sqrt{\sigma^2_{\langle i_n{}^2\rangle} + \sigma^2_{\langle e_n{}^2\rangle}} \tag{7.19}$$

If we take the derivative of the total noise squared, $\sigma_{ENC^2}/\sigma_{ENC} = 2ENC$ and arrange it to give the error on the noise, then the following equation holds true:

$$\sigma_{ENC} = \frac{\sqrt{\sigma^2_{\langle i_n{}^2\rangle} + \sigma^2_{\langle e_n{}^2\rangle}}}{2ENC}. \tag{7.20}$$

7.2.4 Results

These are the results from the simulated noise model. For clarity, each module had its chip temperature normalised at 15 °C and was biased at 150 V. The average values of C_{tot} were calculated using the average of MPI, NIKHEF and Lancaster's results for a stable detector. Each noise value was calculated for a bias voltage of 150 V. Table 7.7 gives a summary of the predicted results. The leakage current for un-irradiated modules is completely negligible as a noise source, but is left in so the model will remain valid for irradiated sensors. The dominant noise sources are the base spread resistance, collector and base currents in the chip; and the strip resistance in the sensor. The total-strip capacitance is a high contributing factor to the noise in the sensor.

	source	dominating par.	Outer	Middle	Inner
Voltage	base spread resistance	R_{bb}	888 ± 18	850± 17	620 ± 13
	Sensor strip resistance	C_{tot}	686 ± 84	631± 77	418 ± 44
	collector current	C_{tot}	615 ± 56	597 ±52	495 ± 29
Current	base current	β	344 ± 50	344 ±50	344 ± 50
	feedback resistance	R_f	292 ± 2	292 ± 2	292 ± 2
	leakage current	T_p	2 ± 0	2 ± 0	2 ± 0
	strip bias resistance	T_p	64 ± 1	64 ± 1	92 ± 1
	ENC		1311 ± 72	1251± 66	947± 40

Table 7.7: The individual noise contributions are displayed, with their corresponding parameters that dominate the term.

Temperature Dependence

The last part of the noise model analysis focuses on the temperature dependence of noise. A simulation using the SCT noise model, calculated the equivalent noise charge over a range of sensor temperatures, from 200 K - 350 K for a general Outer, Middle and Inner module. They were each biased at 150 V. The slope of a linear fit to the predictions gives the noise dependence in ENC/K. The results were compared to the measured noise versus temperature values taken during testing at NIKHEF and CERN. Table 7.8 gives the results.

Module Type	ENC/K	
	Simulated	Measured
OUTERS	4.06 ± 0.18	5.77 ± 0.27
MIDDLES	3.89 ± 0.17	4.85 ± 0.28
INNERS	2.84 ± 0.10	3.86 ± 0.21

Table 7.8: Here the noise model calculated the equivalent noise charge per Kelvin for each module type. A temperature range from 200-350 K was simulated for the sensor temperature of each module. All modules were normalised to have the same chip temperature.

To conclude, for a good understanding of the noise, it is essential to know accurately the value of C_{tot} for each module. This is because the noise is extremely sensitive to even small variations in C_{tot}. The total-strip capacitance of each module however, is a parameter less accurately known with both environmental and time conditions affecting it. The value is also dependent on the set-up used to measure the total strip capacitance. At most, results for nine neighbouring strips have been determined. The SCT specifications set a limit of <1.1 pF/cm for this parameter [6] and [29]. At CERN, a handful of the sensors ($\sim 2\%$) which make up the detector modules were selected from each manufactured group, and their total-strip capacitances measured to cross check that they were well within their specification. They all passed this check. However, not all of these values were recorded in the SCT database. For this reason, the values of C_{tot} are not known for every SCT detector module. They, therefore must be estimated or extracted by some other method. We will now try to correlate the strip capacitance to the total capacitance. The advantage is that it can be measured during detector operation in the ATLAS experiment.

7.3 The role of C_{tot}

At present, before the LHC collisions are to begin, the SCT modules are non-irradiated. The main parameter uncertainty is the total-strip capacitance value for each detector. Since all the depletion voltages are known for each module, this is an ideal opportunity to fix the behaviour of V_{dep}, in order to concentrate on modelling the total-strip capacitance correctly. Experimental noise measurements were made of the detector noise, using thirteen modules of end-cap A. With these noise values, the noise model was fitted to the experimental data outputting a functional form of the total-strip capacitance for each detector. This is very useful, especially since the modules at this moment are not irradiated (and their values are likely to change with the radiation dose).

The data samples presented in this work are for modules that are in a dry environment with a charged detector surface. As discussed earlier, fresh detectors have a much higher total-strip capacitance than those which have been biased for longer. These measurements are not ideal in the sense that during ATLAS running, the modules will have been biased for a longer period of time and will therefore have an uncharged detector surface and a nominal capacitance value. However, by understanding extensively the total-strip capacitance measurements of these results, a comparison can be made to the other fresh detector capacitance measurements taken at Lancaster. This helps build up a complete understanding of the module noise and parameters. This method of extraction would provide useful results if performed at the beginning of the detector lifetime when the modules are stable. It gives an ideal reference data set in order to keep track of the changing module characteristics.

To model the bias dependence of the total-strip capacitance, we have looked for a function to describe the shape of the curves presented in Lancaster's data from Figure 7.5. For a W21 sensor from Lancaster, a fit is made to the measured data points of the curve. A linear plus exponential function fits well:

$$C_{tot} = f(V_{bias}) = a + b \times V_{bias} + c\, exp \left\{ \frac{V_{bias}}{d} \right\} \tag{7.21}$$

where the four free parameters *a, b, c, d* are extracted by the least squares fitting method. Figure 7.7 shows the results. The nominal value of the total-strip capacitance is the C_{tot}

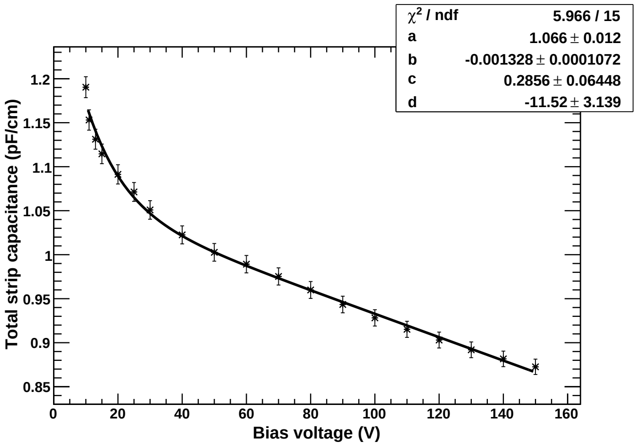


Figure 7.7: A linear plus exponential is fit to the C_{tot} data for a W21 wafer from Lancaster.

value taken at the point where the voltage equals 150 V (C_{150} value). The above expression given in Equation 7.21 for the inter-strip capacitance is substituted into Equation 7.16, along with Equation 7.12. This gives the noise in equivalent noise charge as a function of the bias voltage.

7.3.1 Setup and procedure for taking measured data

In November 2006, the SCT and TRT end-caps were integrated together in the surface reception area (SR1) at CERN. The top left octants of all discs were read out in a noise scan to check that there were no changes in the noise after integration. On Endcap-A they were located in the top left octant of disc 6 and consisted of 5 outer modules, 3 middle modules and 5 inner modules. The bias voltage initially set to 150 V and then decremented in steps of 10 V to a final value of 10 V.

The cooling plant was operated at a back pressure of 4 bar, providing a coolant temperature of approximately zero degrees, resulting in $\sim 15°$C hybrid temperature. The end-cap was continuously flushed with dry air and frequent flushing of nitrogen at a rate of 300 litres/hour providing a dry atmosphere for the modules. The measurements were taken at a relative dew-point of $-25°$C. Under these conditions, as explained earlier, the stabilisation time for the total-strip capacitance was of the order of days. The detector modules had only been biased for a few hours during the course of the testing, and therefore are regarded as fresh detectors.

The depletion voltage, V_{dep} was measured for each sensor at the manufacturer. Their values were extracted from the SCT production database. An average of the wafer depletion values that make up each detector were calculated for each module and used in the model. Table 7.9 gives these values as well as the bias voltage, hybrid temperature and leakage currents recorded during the measurements. A script created an input file for each module containing the information from Tables 7.6 and 7.9 as well as the average measured module noise. In the fits a, b, c and d were left free, with all other parameters fixed. The chip rms noise values were taken as the error uncertainty of the noise. This was then scaled by a factor, k, to give a chi-squared value equal to one.

Module Type	Module number	V_{dep}	T_{hyb}	I_{leak}
		(V)	(°C)	(nA)
6A-TL-O1	20220130000505	60.0	13.4	8
6A-TL-O2	20220130000376	60.3	12.7	43
6A-TL-O3	20220130000506	61.7	13.4	23
6A-TL-O5	20220130000507	64.1	13.3	18
6A-TL-O6	20220130000380	53.3	13.7	40
6A-TL-M1	20220390000128	73.1	14.9	21
6A-TL-M2	20220390000133	75.0	14.8	109
6A-TL-M3	20220390000155	57.8	15.6	14
6A-TL-I1	20220281000096	68.5	13.5	33
6A-TL-I2	20220281001180	90.5	14.3	32
6A-TL-I3	20220281000074	99.0	19.7	28
6A-TL-I4	20220281000067	96.0	13.7	213
6A-TL-I5	20220281000098	95.0	13.3	55

Table 7.9: Depletion voltages of each module, averaged over each sensor, extracted from the SCT production database. Columns 4 and 5 give the average recorded value for the hybrid temperature and sensor leakage current.

The total-strip capacitance, as a function of bias voltage, for freshly biased modules varies significantly from one detector to another. This makes it difficult to extract the nominal stable value of C_{tot} for each module giving the fresh detector data set taken in November 2006. However, C_{tot} measurements taken at Lancaster for fresh detectors will provide a good comparison to the results of the noise fit. An extraction of C_{tot} from future noise measurements for stable detectors would provide a very useful data reference set for unirradiated modules.

7.3.2 Statistical error on the noise

The statistical error for each noise measurement taken at independent bias voltages is derived from the standard deviation:

$$\sigma^2_{ENC} = \frac{\sum_{i=0}^{N} (X_{ENC} - \mu_{ENC})^2}{(N)} \tag{7.22}$$

where X is the measured chip noise and μ is the mean noise value of N chips per module. This typically gives an error on the noise between 10-30 ENC for each data point. By using these errors, the chi-squared value of the fit returns a very small number, which implies that the errors have been wrongly estimated. In order to determine the errors to each parameter in the fit more accurately, a scale factor k is introduced into the error to give the following:

$$\chi^2/NDF = \frac{\sum_{i=0} (Y_{obs} - Y_{exp})^2}{(k \times \sigma_{ENC})^2}/NDF \tag{7.23}$$

where Y_{obs} is the measured noise data point, Y_{exp} is the value of the fit and the k factor is the value at which $\chi^2/NDF \approx 1$.

7.3.3 Results

Figure 7.8 shows examples of the noise as a function of bias voltage. The bias voltage is along the x-axis and the noise (in equivalent noise charge-ENC) on the y-axis. The line is the final result of the fitting using the noise model. As can be seen, the fit describes the data points very well.

The next set of results shows the output form of the total-strip capacitance that best described the measured noise points. Figure 7.9 gives these results and includes also the functional forms of the strip to strip capacitance and strip-to-backplane capacitances using Equation 7.14. On the x-axis is the bias voltage in Volts and on the y-axis are three capacitance curves. The top curve is C_{tot}, the middle curve is two times the strip to strip capacitance and the lower curve is the strip to backplane capacitance. All capacitances are given in pF/cm. The output form follows the expected trend, showing that the total-strip capacitance decreases with applied bias voltage. Compared to Lancaster's fresh detector measurements, the capacitances are slightly higher. However given the fact that the amount of excess capacitance charge for each detector varies significantly from one another, this is not surprising.

The extracted C_{150} values from the noise simulation, show that the inner modules tend to be higher, confirming the results found at the other institutes. The range of values for C_{150} were 1.04 - 1.13 pF/cm for outers and middles, and 1.15 - 1.29 pF/cm for inners.

Since the main uncertainty in the noise model is the current gain of the ASIC, the extraction method was rerun for the central value of $\beta \pm \sigma$. Then the fractional errors were added in quadrature to give an overall error on C_{150}. Table 7.10 gives a summary of the fit values for parameters a,b,c,d for each module with their associated values of C_{150}. The error in C_{150} is marginal given the large spread of the current gain. This significantly demonstrates that the capacitance value does not depend on this parameter.

Using the data set from November 2006 it is difficult to assess the complete accuracy of the noise model. The main uncertainty is the knowledge of the total-strip capacitance. A method of extracting it for sensors with known depletion voltages has been developed and shown to work well with a linear plus exponential dependence on the bias voltage. The extracted values of the total-strip capacitance from the model show that for each module type the spread is very small. If these measurements are compared to the fresh sensor capacitance measurements from Table 7.4, then they are approximately 18% higher. Lancaster's fresh sensor measurements compared to the stable sensor measurements are approximately 20% higher.

It is also known that once the sensors are biased for a long time, their total-strip capacitances will stabilise. The noise is affected by the total-strip capacitance between all strips on a sensor (768) and not just two nearest strips as was measured by all institutes. The values extracted from the model are thus expected to be higher than those of MPI, NIKHEF and Lancaster. The total-capacitance values extracted from the model are therefore quite accurately determined and incorporate the total-strip capacitance seen by the amplifier. For accuracy and as an initial reference set, it would prove very useful to extract each module's total-strip capacitance using this noise method.

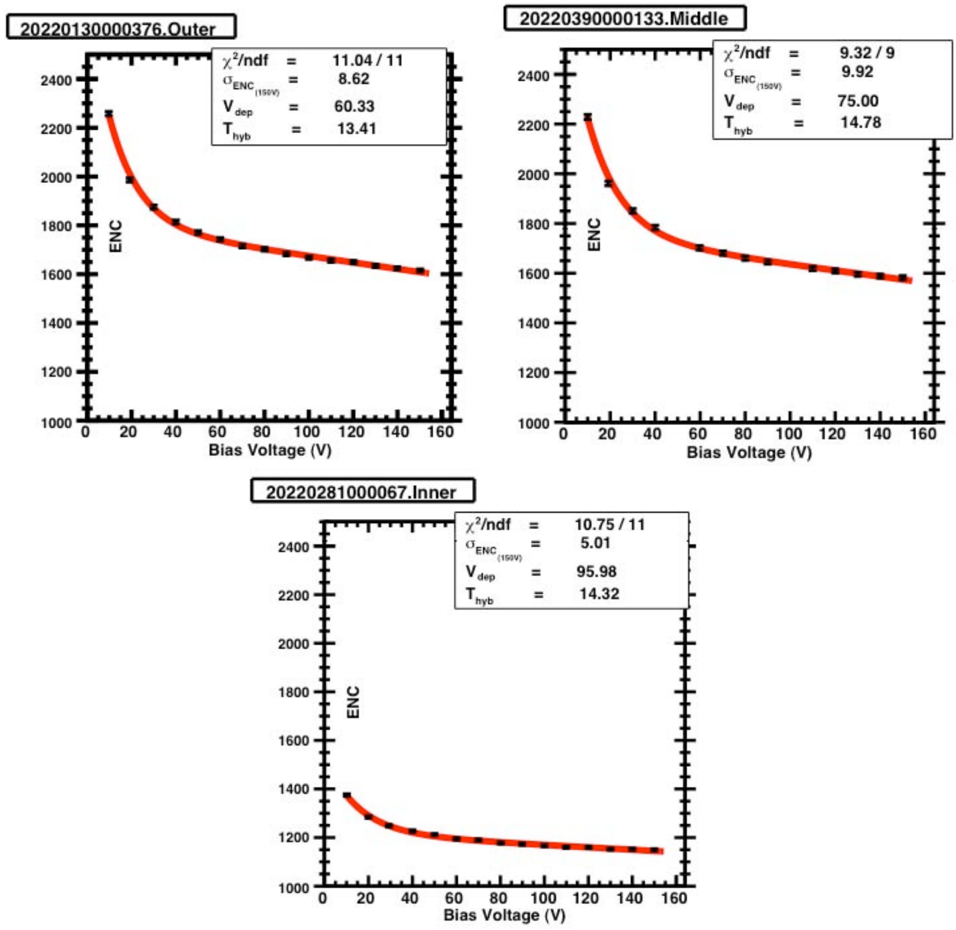


Figure 7.8: These are the noise fitting results for one outer, middle and inner module, whereby the total-strip capacitance is required to have a linear plus exponential functional form. The points are the measured data and the line gives the noise model value. The error on the noise, σ_{ENC} is quoted for the 150 bias voltage measurement.

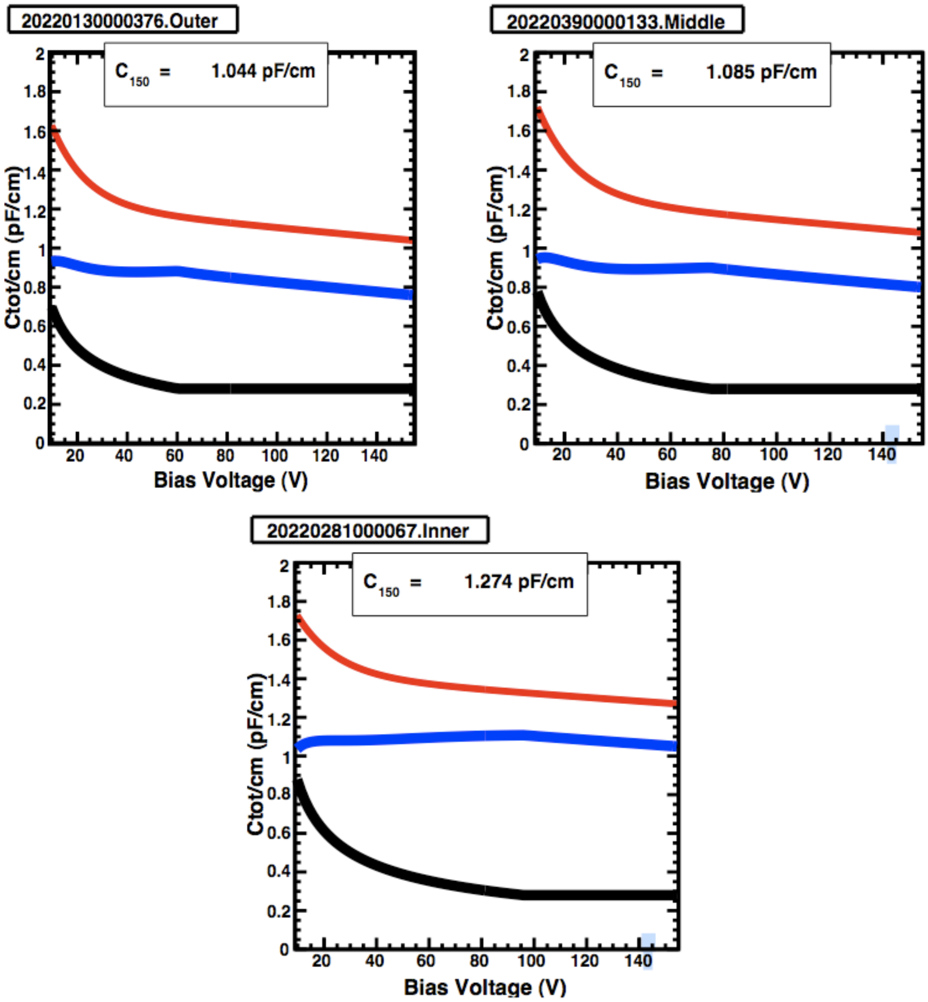


Figure 7.9: The output results for the capacitances from the noise fitting for one outer, middle and inner module. In red (upper curve) is the total-strip capacitance, blue (middle curve) is two times the strip to strip capacitance and in black (lower curve) the strip to back plane capacitance.

FRESH detectors					
Module type	a	b	c	d	$C_{150}(pF/cm)$
O1	1.51E-11	-1.47E-14	1.04E-11	-13.73	1.04 ± 0.02
O2	1.56E-11	-1.22E-14	6.38E-12	-23.1	1.12± 0.02
O3	1.64E-11	-1.63E-14	1.07E-11	-14.9	1.13 ± 0.02
O4	1.55E-11	-1.38E-14	9.89E-12	-15.15	1.09± 0.01
O5	1.58E-11	-1.42E-14	9.67E-12	-15.7	1.11 ± 0.01
M1	1.50E-11	-1.59E-14	1.07E-11	-14.85	1.10 ± 0.02
M2	1.46E-11	-1.38E-14	1.04E-11	-14.83	1.09 ± 0.02
M3	1.65E-11	-2.77E-14	1.15E-11	-10.69	1.07 ± 0.02
I1	8.49E-12	-5.95E-15	3.78E-12	-14.40	1.23 ±0.05
I2	8.75E-12	-6.03E-15	3.71E-12	-15.11	1.27± 0.05
I3	7.68E-12	-7.30E-16	2.34E-12	-57.58	1.29 ± 0.05
I4	7.90E-12	-5.57E-15	3.30E-12	-13.97	1.15 ±0.06
I5	8.36E-12	-6.41E-15	3.93E-12	-14.4	1.20± 0.05

Table 7.10: A summary of the fitted parameters a, b, c, d and extracted values for the total-strip capacitance at 150 V using Equation 7.14.

7.4 Conclusions and Outlook

A noise model has been tested with measured noise results for thirteen SCT modules. A simulation gives a breakdown of the overall contributions to the noise. The dominating source is the noise in the amplifier due to the base spread resistance. The total-strip capacitance is the dominating factor in the sensor. A fit has been made to the measured data points with the best fit outputting the functional form of the total-strip capacitance. A method of constraining the C_{tot} behaviour has been investigated and the results favour a linear plus exponential form. Performing such a fit on all SCT modules, gives a good approximation of the geometrical values of C_{tot}.

It would also be useful to study the radiation dependence of other parameters. For example the total-strip capacitance is known to increase with radiation dose and the current gain β of the chip is expected to degrade. This causes an increase in parallel noise in the front-end, as a result of an increase of shot noise in base current. These changes would need to be considered in the future.

A sequence of noise scans at bias voltages from 30-150 V in 20 V steps would be sufficient for an initial estimation of C_{tot}. Further scans later in the year should be implemented in order to determine V_{dep}. The accumulated radiation dose is also needed for investigating the total-strip capacitance and current gain.

As modules suffer radiation damage, the depletion voltage will change. Knowing the total-strip capacitance, the depletion voltage parameter can be released from the noise model, allowing it to be extracted. This could provide an extremely useful method for tracking the radiation damage of the detector and giving an overall estimate of the lifetime of the detector. For the purpose of monitoring the radiation damage, this method for extracting the depletion voltage would be most useful if performed several times a year. This method is only useful however, if firstly the geometrical total-strip capacitance value is known for all modules before irradiation. The detector commissioning phase in 2008 would be an ideal opportunity to measure these.

CHAPTER 8

COMMISSIONING WITH COSMIC MUONS

"The Heart of ATLAS"

CERN courier, April 2006

Contents

Cosmic rays are particularly useful for commissioning purposes of the ATLAS detector. Cosmic muons provide an initial test of the various aspects of the detector, allowing it to acquire real data hits for the first time. The offline software used to reconstruct the data gives information on noisy channels, calibration and alignment as well as the synchronisation between the different sub-components. Cross-talk between modules and noise resulting from synchronous running of detectors can also be investigated. These commissioning periods are essential for successfully integrating all systems together.

The installation of SCT in the heart of ATLAS has been completed in the beginning of 2008. In March 2008, the barrel participated for the first time in a global ATLAS "milestone" run, M6. Many of the sub-detector components were switched on during this week, allowing cosmic particles to be tracked from the SCT right through to the muon chambers. This chapter will discuss the monitoring package implemented for the SCT, as well as a discussion on the results obtained from its use during the M6 run.

8.1 Cosmic Muons

8.1.1 Cosmic muons at the surface

Cosmic rays originate from outer space, and strike the earth from many directions. They are composed essentially from all the periodic elements, but 89% of nuclei are hydrogen,10% helium and 1% heavier elements [64] . When cosmics enter the upper atmosphere they collide with the atoms and produce a shower of secondary particles which, in turn, make their way towards the surface of the earth. They lose their energies by ionisation and radiative processes such as *Bremsstrahlung*, *pair production*, and photo-nuclear interactions. Most cosmic rays at sea level are muons with a mean energy of $\approx$ 4 GeV.

For cosmic muons, below 1 GeV the energy spectrum is almost flat, it then steepens gradually to reflect the primary spectrum $\propto E^{-2.7}$ in the 10-100 GeV range. The angular distribution of muons at the surface is $\propto \cos^2\theta$, where θ is the zenith angle. At lower energies the angular distribution becomes steeper, whilst at higher energies it flattens and approaches a $sec\ \theta$ distribution. The Particle Data Group [64] surface flux approximation gives:

$$\frac{dN_\mu}{dE_\mu} = \frac{0.14E_\mu^{-2.7}}{cm^2 \times s \times sr \times GeV} \times \left\{ \frac{1}{1+\frac{1.1E_\mu \cos\theta}{115GeV}} + \frac{0.054}{\frac{1.1E_\mu \cos\theta}{850GeV}} \right\} \tag{8.1}$$

The two terms give the contributions from charged pions and charged kaons. The contributions from charm and heavier flavours are neglected using the above approximation. The total flux per unit horizontal area was taken to be 130 muons per square meter per second.

8.1.2 Track Reconstruction

Co-ordinate system

In ATLAS, the z-axis is defined as the direction of the beam and the plane transverse to the beam is the x-y plane (making a Right-Handed Cartesian co-ordinate system). Pointing into the centre of the LHC ring is the positive x-axis and the positive y-axis is pointing upwards. Three variables which are important with regards to trajectories of particles are ϕ, θ, η:

- ϕ = azimuthal angle measured around the beam axis;
- θ = polar angle measured from the beam axis;
- η = pseudo rapidity defined as -ln tan$\left(\frac{\theta}{2}\right)$.

Other variables which are defined in the x-y plane and which are also useful to know are: the transverse momentum P$_T$, the transverse energy E$_T$, and the missing transverse energy E$_{Tmiss}$.

The trajectory of a charged particle in a static, uniform, magnetic field, in a vacuum is a helix. Five parameters suffice to define such a helix. ATLAS uses the following parametrisation, with all variables defined at the point of closest approach to the beam axis, x = 0, y = 0. The parameters in the x-y plane are as follows:

- $\frac{1}{P_T}$ = Reciprocal of the momentum component perpendicular to the z-axis;

- ϕ = Azimuthal angle;
- d_0 = Transverse distance to the beam axis.

The parameters in the R-z plane are:

- $\cot\theta$ = Cotangent of polar angle, whereby $\cot\theta = \frac{P_z}{P_T}$;
- Z_0 = Longitudinal impact parameter, defined as the z-position of the track at the point of closest approach.

The detector is labelled with two sides, A and C, and a barrel section B. Side A has z > 0 and side C has z < 0; these are at either end of the barrel region.

A framework called `ATHENA` [7], based on the `GAUDI` [60] framework from LHCb, serves as the software developed by ATLAS users. The framework encourages a common approach, allowing developers to integrate their code into the existing C++ skeleton. It provides the tools necessary for common functionality and communication between the different software components. The framework structures applications such as particle generation, simulation, reconstruction, analysis into a series of algorithms. The applications are managed through Python “jobOptions” files which allow users to load specific libraries of algorithms, specify the order in which the algorithms are executed, as well as configuring each algorithm’s behaviour.

The ATLAS source code is organised into ’packages’, which can consist of several algorithms. Each algorithm has access to a number of services. These can include, booking and histogramming data, reading in event data, acquiring information on the detector and logging messages output from an algorithm. The packages exist in a CVS repository where they are assigned versions using tagging. Code management organises the code. A requirements file specifies details on which packages to build and the details on how to build them.

Figure 8.1 gives an overview of the stages of the Inner Detector track reconstruction. To simulate the detector response, the geometry and its description with `GEANT4` is used.

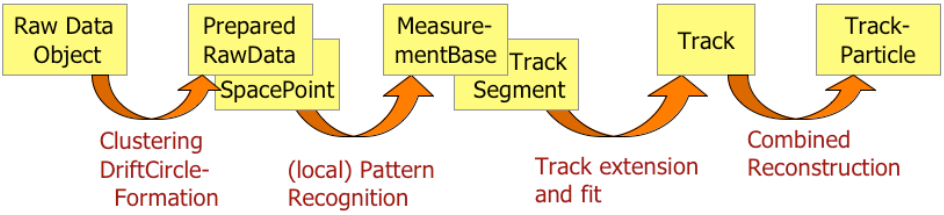


Figure 8.1: A schematic of the stages of Inner Detector track reconstruction.

When a particle passes through a detector volume, a hit is generated according to the energy deposit. Next the hit needs to be digitised so that its data form is the same as that of a real hit, registered by the module front-end electronics. The digitisation package includes charge sharing and cluster formation. This output is called the Raw Data Object (RDO), which is the standard format the reconstruction software needs in order to interpret the data. For the real data hits, a Byte Stream converter decodes the data fragment from the DAQ into an RDO.

The on-detector electronics create the cluster of hits before sending the event data off detector. After the byte-stream conversion of this event, a 32-bit identifier is created which corresponds to the first strip of a cluster and the number of associated hit strips, giving the cluster width. Next the clusterisation algorithm loops over the channels in a cluster and cross checks them against the channel information in the conditions data base. Any bad channels, i.e. noisy or dead, are removed from the cluster. It can also be the case that a bad channel is removed from the center of a cluster, dividing it into two separate clusters. These clusters serve as the input for forming space-points, which are strip pairs formed from overlapping strips on opposite sides of a module. The pattern recognition software uses these spacepoints to find suitable track candidates. The number of modules containing spacepoints for a possible track candidate is counted. The tracking is based on the global fitter used in the combined testbeam. The track fitting tries to fit the first three spacepoints. If that works, it then proceeds to fit the fourth spacepoint. It can sometimes occur that only one side of a module is hit by a cosmic muon. In such a case a spacepoint would not normally be reconstructed. To account for this, a track candidate will be extrapolated to the module which contains a one-sided hit. If the hit strip is closer than 0.7 mm to the track, it is added to the track hits. The minimum number of spacepoints for a track candidate is 4 or in the case of a one-sided hit, 3 spacepoints + one strip. The final track fit uses the clusters associated to those spacepoints, to perform the final track fit. The channels associated to the final reconstructed tracks are called Reconstructed Input Objects (RIOs). Since the cosmic rays do not originate from the centre of the detector, where normally the particle collisions would take place, a point high in the sky is used for the reconstruction of spacepoints. Therefore the tracking algorithms were changed so as not to include any vertex constraints.

Another factor to be incorporated into the tracking for the cosmics is the timing. The cosmic muons arrive at random times, while the default reconstruction software assumes that the particles arrive synchronously with the readout clock. The reconstruction software was modified for the cosmics such that it calculates the difference between the readout clock and the arrival time of the muon.

8.2 SCT Monitoring

The SCT monitoring software is an offline package, but it can also be run online at the event filter stage of the triggering process. In this way, the detector performance can be monitored and a check made of the data quality before the events are written to disk. An Online Histogram Server collects detector data of the reconstructed objects. For example, raw data information, track parameters, silicon space-points and clusters. Then using a graphical interface known as the Online Histogram Presenter, data can be monitored continuously for quality control. To have a visual check of the tracks in a certain event, the ATLAS event display, ATLANTIS [8], can also be run both online and offline. The next section will now discuss the monitoring package developed for the SCT, followed in more detail by the Noise occupancy tool. Using the first cosmic data in the ATLAS cavern, the SCT performance was tested. This will be discussed later on in the chapter.

The SCT monitoring code is developed within the `ATHENA` framework. It is based upon the initial monitoring code written for the combined test beam as well as several tools that were developed within the track reconstruction software. The aim of the monitoring is to provide a set of histograms that can summarise the main characteristics of the SCT data. These histograms represent the detector performance such as occupancies, noise and module efficiencies. Its use will determine any potential problems within the SCT including inconsistent data, channels which are dead or noisy and inefficient or unstable regions of the detector.

The monitoring tool which can run both online and offline also provides access to module information from the conditions database implemented in COOL [10]. The tool also allows a summary of the monitoring results to be written to the database.

8.2.1 Overview

The package consists of several tools, each performing its own monitoring task. To date, there are five different types of tools which monitor the data. More than 150 histograms summarise the event data and over 8000 individual hitmaps are generated. The main algorithm calls each tool in turn, running three methods each time:

- **initialise**- During this method the various histograms used in the monitoring are booked;
- **execute** - This is performed for each event, performing analysis on RDOs and filling the histograms. They are sent periodically to the Online Histogram Server;
- **finalise**- Any output summarising the run is performed here.

Now a brief overview of these five tools will be presented.

Hits

Histograms of the raw data hits and cluster sizes are created. These can be in 2-D map format for η versus ϕ or individual 1-D histograms for each side of a module. The SCT timing can also be checked with the histogram of time bin versus hits.

Tracks

This contains information on the quality of the tracks. As mentioned previously, the SCT software uses spacepoints to find suitable track candidates during the pattern recognition. Once the track is fitted, the raw hits in the track are compared to those in the reconstructed track. The residual is defined as the distance between the raw hit and the hit on the track. The residuals use the X co-ordinate in the local frame of the module. They represent one form of measuring the track quality. Another method is to calculate the pull distribution from the residuals. This is defined as the residual divided by the combined errors on the track and raw data hits.

$$p = \frac{X_{track} - X_{hit}}{\sqrt{\sigma_{track}^2 + \sigma_{hit}^2}}$$

Errors

This tool checks any errors caused as a result of the raw data being sent to the ROD and converted into a common ATLAS event format.

Noise occupancy

This tool creates 2-D η - ϕ maps of the module noise occupancies. The author of this thesis added to the development of this tool, to implement a less biased, more efficient manner for calculating the noise occupancy. This tool will be discussed in more detail in the next section.

Hit efficiency

When a track has been fitted to the raw data hits in an SCT cluster, the perigee parameters for the track are determined. In the case of cosmics when there is no magnetic field, this will simply be a straight line. Using these parameters the track is extrapolated back through the surfaces of the silicon part of the Inner Detector and the number of sensitive detector elements crossed by the track without inducing a signal in these elements is determined. Every such occurrence is called a hole. In order to differentiate between hit inefficiencies and pattern inefficiencies a search is performed around 1mm for clusters around holes. Figure 8.2 shows a schematic for a hole and an unassociated cluster on a track.

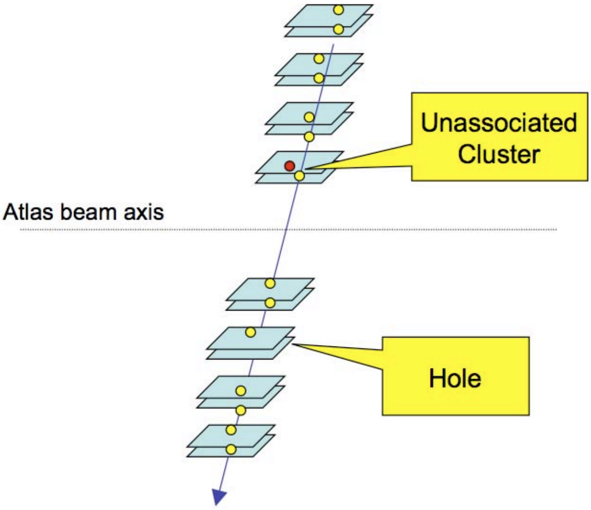


Figure 8.2: Schematic describing a module inefficiency and unassociated cluster.

8.2.2 `SCT HitsNoiseMonTool`

This tool incorporates the information for both hits and noise related to an event. Previously they ran as two separate tools, but now they are combined to make the code run more efficiently. The noise occupancy calculation has been improved upon due to several aspects needing refinement. Firstly the time needed to execute the noise occupancy calculation needed to be reduced. Also, the method to calculate the noise occupancy was developed to calculate it at strip level as opposed to module level. The last improvement involved using cluster hits associated to spacepoints instead of only the reconstructed hits on a track.

The original method for calculating the noise occupancy has been described in [74]. This method performs the noise occupancy calculation by looping over the number of raw data hits output from the modules and counting the number of 'X1X' hits in the event. Where the three characters denote the previous-present-next bunch crossing during readout. For every event it retrieves the track collection and RDO collection, filling 2D histograms in η and ϕ of RIO hits and X1X hits. Once a given run is finished, the difference in the RDO hits and the X1X gives the number or noise hits in all the events. Then this value is averaged over all strips in a module and the number of events to give an average noise occupancy per module side.

$$\frac{1}{N_{events}} \times \frac{1}{N_{strips}} \sum_{events} (\mathrm{Total}_{\mathrm{X1X}} - \mathrm{Total}_{\mathrm{RIO}}) \tag{8.2}$$

The method to calculate the noise occupancy was improved by using the cluster of hits belonging to the space points in an event. Previously only hits associated to a reconstructed track were used. This method was somewhat biased since a track is only reconstructed if there are a minimum of four space points in the fit. There may be events where only one or two space points are present, therefore it was decided to implement the calculation using space points for a less biased noise occupancy value. It could happen that two noisy strips on a module both fire at the same time, giving a falsely made space point. It is for this reason that the method is only less biased and not completely unbiased. Instead of calculating the occupancy at module level, the space point method calculates it at strip level. Any hit strips will be removed from the number of strips in one module side for each event, in comparison to the previous method which only took the strip average at the end of all the events.

$$\frac{1}{N_{events}} \times \sum_{strips} \frac{(\mathrm{Total}_{\mathrm{X1X}} - \mathrm{Total}_{\mathrm{RIO}})}{\mathrm{N}_{\mathrm{strips}} - \mathrm{Total}_{\mathrm{RDOfromSP}}} \tag{8.3}$$

The spacepoint method begins by retrieving the spacepoint collection for an event. It loops through it to find the number spacepoints and the cluster of hits associated to the space point (RDOfromSP). A vector is formed containing the module identifier and the cluster hits in an event. The method which forms the general histograms of the package was modified to make a similar vector containing the raw data hits and identifiers using the raw data collection. At each event, each module has its occupancy calculated using equation 8.3. In comparison to the track based method which looped over the same data collections twice during the calculation, the space point method decreased significantly the time needed to execute the monitoring calculations per event. At the end of all the events, the total summed occupancy was divided by the number of events giving the average occupancy in each module.

One of the main problems with the monitoring code was the amount of time needed to execute the code at each event. The space point method managed to reduce the execution time from 700 ms to 400 ms. Further changes to the various monitoring algorithms have reduced this time to only 90 ms per event.

8.3 Milestone Runs

At the beginning of March 2008 for one week, the SCT barrel had the opportunity to commission both the hardware and software using cosmic rays. Above the ground, the barrel ID had been tested using cosmics in the SR1 building successfully. In the ATLAS cavern, this was the first time the SCT could join a global detector run.

8.3.1 Set-up

Three triggers were used during the M6 run. The tile calorimeter, the muon barrel resistive plate chambers, and a scintillator trigger specifically for the ID. Primarily the ID trigger was used, consisting of two scintillators placed above the muon chambers on level 8 in the ATLAS cavern. They were 144 cm $\times$ 40 cm $\times 2.5$ cm and positioned $\sim$ 1 meter apart. Figure 8.3 shows a schematic of the ID scintillator trigger. Since the area of the scintillators is relatively small, a trigger rate of approximately 1 Hz was achieved. In order to have optimal charge collection efficiency it is essential to have a stable trigger time for the TRT and SCT detectors.

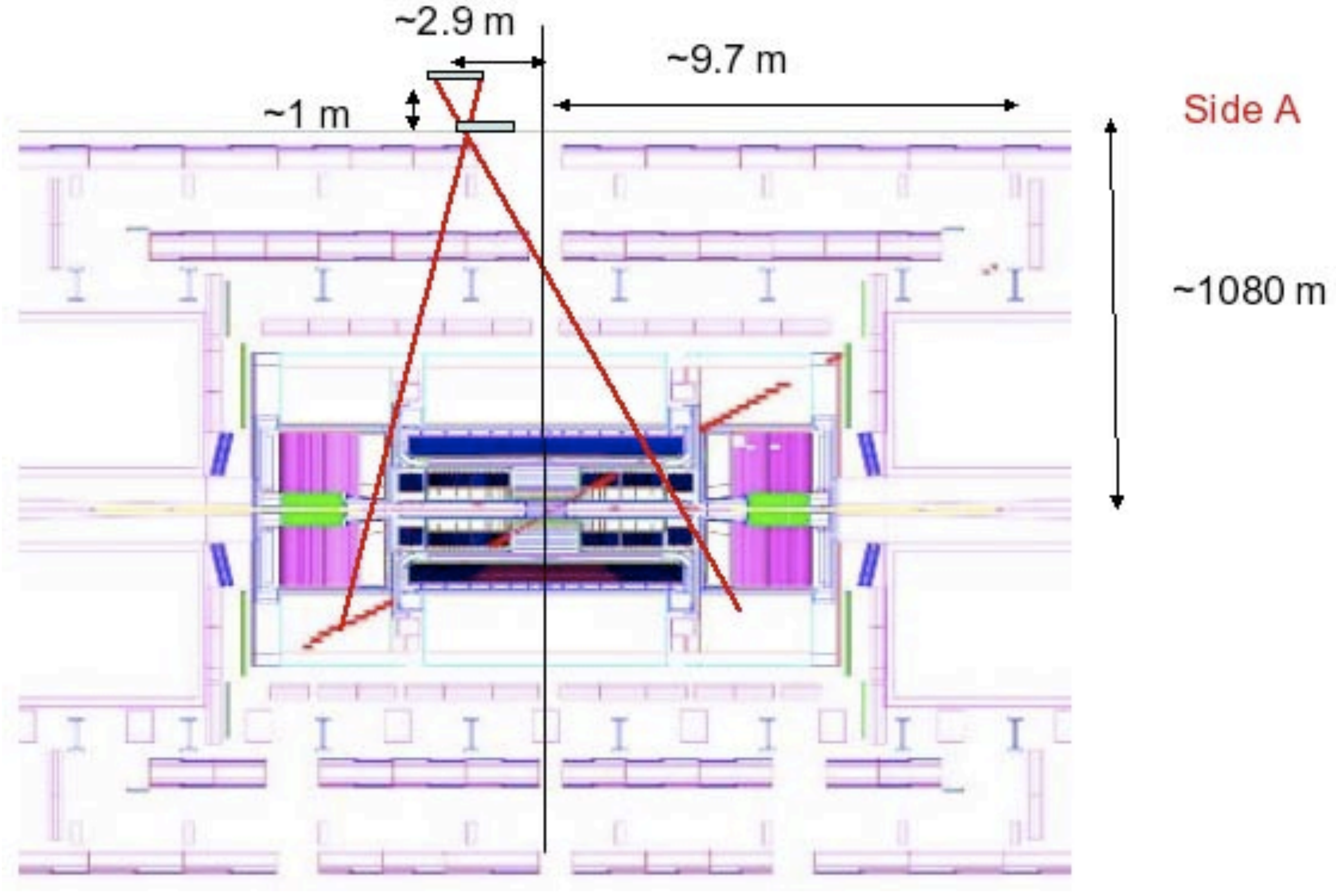


Figure 8.3: Schematic showing the ID scintillator placed above the muon chambers of the ATLAS detector.

8.3.2 Timing

During beam physics, the SCT system clock will be synchronized to the bunch crossing clock cycle. However, for cosmics, the arrival of the particle is random with respect to the system clock cycle. It is therefore necessary to measure the phase of the trigger with respect to the 40 MHz system clock. First, the clock and command signals of all the modules were synchronised to arrive at the same time. This is necessary, since compensation must be made for the different propagating delays of the signals from the timing electronics to the modules. Next, the SCT is timed in properly to ensure the readout of the correct event to maintain a synchronised Bunch Crossing ID. A course delay is initially varied (in 3 clock cycle steps) and a peak in the number of coincidences versus timing offset gives the approximate timing. Then a fine delay tunes the relative bin occupancies further (280 ps level), optimising the hit efficiencies. For the M6 run, only the course delay was used.

8.3.3 Runs and Tests

A large fraction of the SCT barrel detector was tested (1962 modules) during the cosmic commissioning runs. The TRT barrel also participated with three octants readout during tests. A technical pre-M6 run allowed the SCT integration into the ATLAS readout and control, in preparation for the M6 week. The modules corresponding to all four cylinders of the SCT barrel were present in the run, except for those modules linked to three cooling loops equating to 48 × 3 modules. Two types of runs were made:

- A “cosmics” run where modules were triggered to be readout by a passage of a muon going through the trigger;
- A “noise” run where all modules were triggered simultaneously by a pulse of fixed frequency.

The cosmic runs consist of hits that are both real and noise. Whereas, for the noise runs, the detector is not timed in, and the likelihood of having a muon passing through the detector during readout is much less.

During the M6 run, there were several successful runs which allowed the detector and tracking performance to be monitored. The SCT was triggered at different rates (ranging from 8-100 kHz), looking for any differences in noise measurements. Then a number of global ATLAS cosmics runs were taken. Run 41912 was a reference noise run taken for the SCT with a 1 fC threshold using 100 kHz triggers with the modules in an any hit, expanded readout mode. Two good cosmics runs with a number of tracks were taken; 42325 and 43719. The timing was optimised to a +20 clock cycle. The modules ran in any hit, expanded mode with a 1.0 fC threshold, using a combination of scintillator and tile triggers with a trigger rate of less than 1 Hz. Below is a summary of the different detectors involved in each of the cosmic runs.

42325: TRT | Tile | CTP | TDAQ | MDT | SCT | LVL1

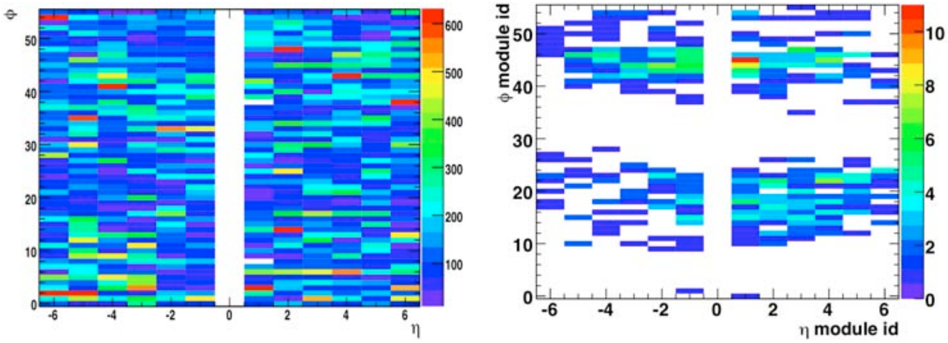
43719: TRT | Tile | TGC | CTP | TDAQ | MDT | SCT | LArg | RPC | HLT | LVL1

For the main cosmic analysis, the results will be focused on run 43719, since more events were available for this data set. During this particular cosmics run, more than 1200 tracks were present in the SCT, of which 1183 were present also in the TRT. The results will now be presented.

8.3.4 Results

Hits

Maps containing the raw data hits (RDOs) and reconstructed hits (RIOs) were created for run 43719. The maps use only the events in which there was a track going through the SCT. The RDO maps contain all the hits readout in each layer of the barrel. These hits contain both real hits due to cosmic tracks and hits due to noise, with the noise hits dominating overall. On the x-axis is the η position of the module and on the y-axis is the ϕ position of the module. On average there were approximately 550 hits per event with four space points per event. Figure 8.4a shows an example RDO map for Barrel 6, side 0, and Figure 8.4b gives the corresponding reconstructed hits associated to the created spacepoints. As one can see, there are a number of modules which are immediately recognisable as being more noisy than the others. These are denoted by the green, orange and red colours in Figure 8.4a. During this run, the information on each module using the conditions database [9] was unavailable. Therefore modules that were unbiased or had tripped as well as defective strips such as dead, stuck or noisy have all been included in the maps as well as in the calculations of hit efficiencies. In future runs, the conditions database will inform the monitoring algorithms of these module defects, so they can be removed from the calculations.



(a) (b)

Figure 8.4: (a) shows the raw data hits observed in module side 0 of Barrel 6. The hits represent both real and noisy hits. (b) shows the reconstructed hits associated to tracks in Barrel 6, side 0.

Tracks

The cosmics were reconstructed using the global χ^2 fitter [26]. Using the parameters associated to the track fit, distributions of $\eta, \phi, \mathrm{d0}$ and z0 of the tracks in the SCT were histogrammed. Figure 8.5 shows the results. The double peaks in $\eta, \phi, \mathrm{d0}$ are due to a combination of the different triggers being used in the run. The left most peak in $\eta, \phi, \mathrm{d0}$ corresponds to the ID scintillator trigger and the right distribution represents events triggered on the muon RPCs. Most of the events in which a track crossed the SCT were one track events. There were, however, some which contained more than one track, with one event containing 4 SCT tracks. Figure 8.6 shows the number of reconstructed hits for all the one track events. Figure 8.7 shows two different events in which tracks went through the SCT barrels. The ID solenoid and toroids were both switched on during some later cosmic runs, causing tracks to be deflected through the subdetectors. Figure 8.8 shows some nice events where curved tracks are present.

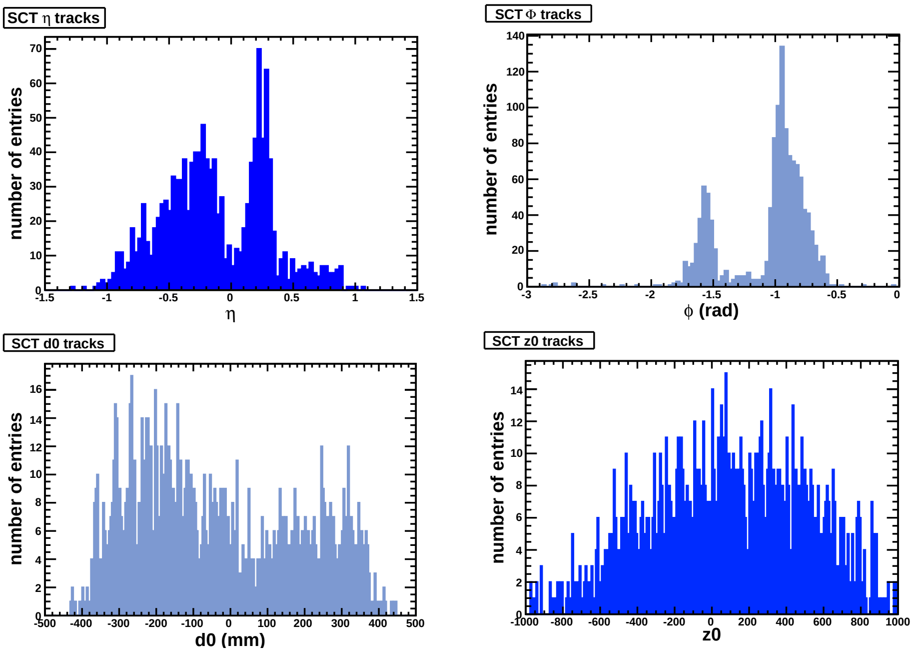


Figure 8.5: Track parameter distributions of η, ϕ, d0 and z0 respectively.

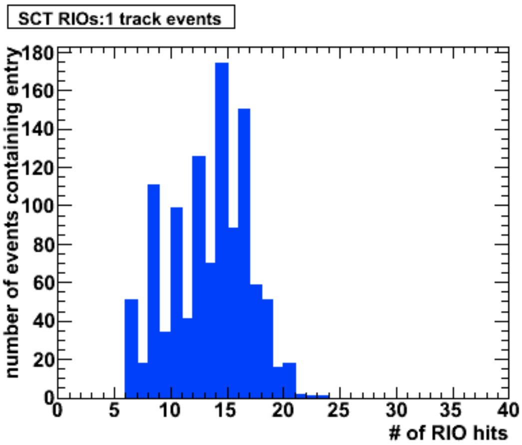


Figure 8.6: The number of reconstructed hits per track for all events containing one track. The number of hits are mostly even since one spacepoint consists of hits in both module sides.

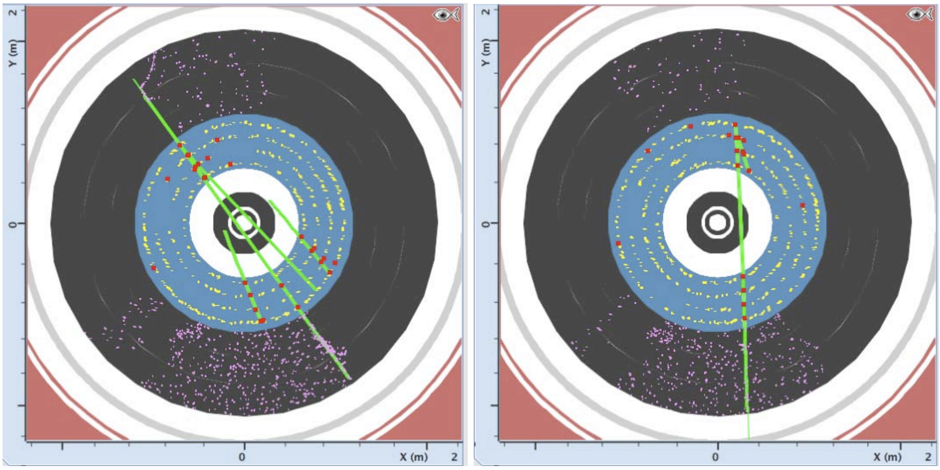


Figure 8.7: Left: An event showing 4 tracks in the SCT barrel, with hits in the SCT and TRT. Right: A cosmic muon going through the upper and lower sector of the barrel SCT.

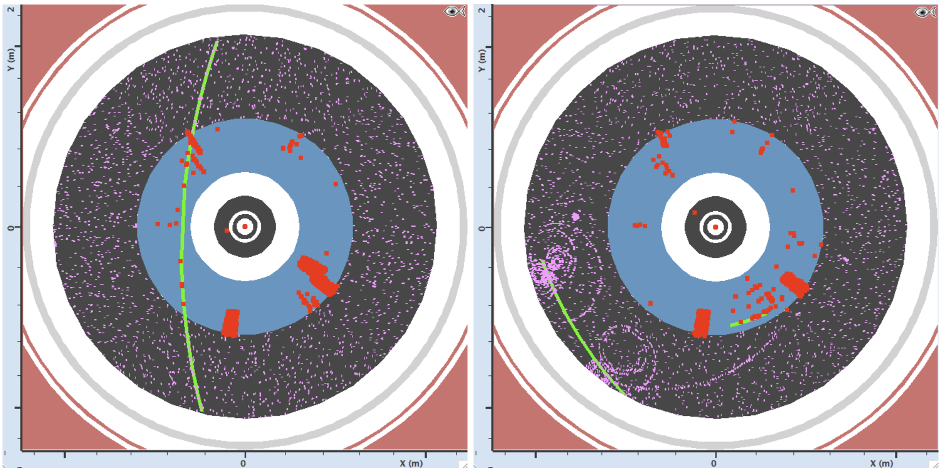


Figure 8.8: Cosmic muons deflected through the Inner Detector with the solenoid and toroid magnets switched on.

Alignment and residuals

Using the track parameters obtained from the reconstruction, a first estimate of the alignment between the TRT and SCT shows promising results (see Figure 8.9). Without performing any alignment fits, a resolution of 0.69 ± 0.04 mrad is found for the difference in ϕ measurements taken from the TRT and SCT ϕ track parameter. Similarly, the spread in the d0 measurements gives a resolution of 444 ± 25 μm. Residuals were calculated for each barrel layer, taking the difference between the x-coordinate of the reconstructed track hit and the cluster hit used in the tracking. Figure 8.10 shows the mean and resolution for Barrel 3, side 0. Values ranging from of 76 - 111 μm are calculated from fitting the data points to a Gaussian. For this run, there were not enough cosmic track events present within the detector, to perform a full alignment on the modules. Without this information, the results for the residuals as well as the hit and tracking efficiencies are subject to lower computed values.

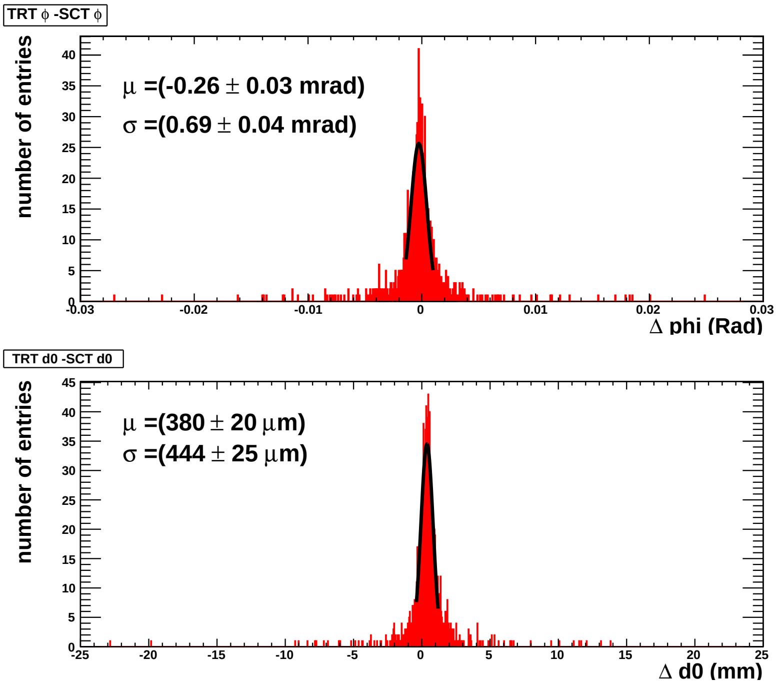


Figure 8.9: A very preliminary result of the barrel alignment comparing the track parameters of ϕ and d0 for the SCT and TRT.

Using another run where the solenoid and toroid magnets were switched on, the residuals for the SCT tracks were re-calculated. There were no significant differences when compared to those without a magnetic field. Table 8.1 summarises the differences in the residuals for each layer with the magnets both off and on.

To compare these values with the nominal design resolutions the following text discusses the main positioning uncertainties. The main requirement for placement comes from ensuring sufficient overlaps between modules to allow precise module-to-module alignment and to minimise holes seen by particles coming from the interaction point. This requirement is most stringent in the transverse R-Φ direction. The placement tolerances are 67, 90 and

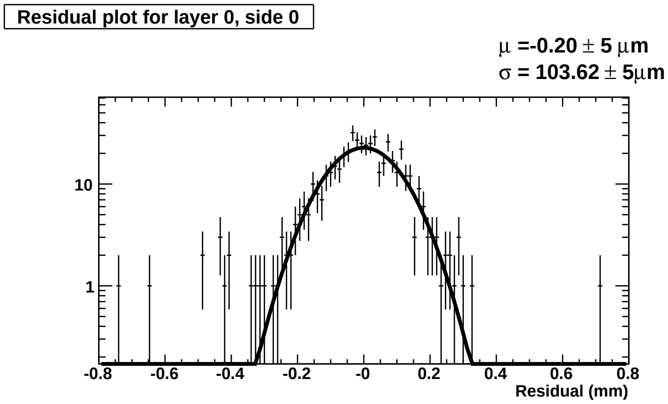


Figure 8.10: Residuals for Barrel 3, side 0 calculated using the x-coordinate of the track and the raw hit.

	Magnets off		Magnets on	
Layer,side	μ (μm)	σ (μm)	μ (μm)	σ (μm)
0-0	0 ± 5	104 ± 5	-10 ± 7	154 ± 12
0-1	4 ± 5	91 ± 5	-1 ± 5	129 ± 9
1-0	5 ± 4	76 ± 3	-15 ± 4	124 ± 7
1-1	-13 ± 5	95 ± 4	-5 ± 4	118 ± 6
2-0	-27 ± 5	105 ± 4	-4 ± 3	99 ± 5
2-1	-31 ± 4	83 ± 3	10 ± 3	95 ± 5
3-0	25 ± 5	106 ± 4	4 ± 4	127 ± 8
3-1	21 ± 5	111 ± 4	3 ± 6	142 ± 12

Table 8.1: A comparison of the residuals with and without the magnets switched on

220 μm for the module placement of Inner, Middle and Outer modules respectively [49]. The placement of discs is 100 μm in x-y and 1000 μm in Z. The actual position of the modules is determined with a high precision from the alignment residuals using particle tracks. This reduces the need for very precise placement of the modules and the support structures. Nevertheless, the better the placement, the more readily the alignment procedures will converge and the easier it will be to understand systematic uncertainties. So from Figure 8.10 and Table 8.1, the values are considered well within specifications.

Noise occupancy

A comparison was made of the noise occupancy measured during noise run 41912 and cosmics run 43719. The results were both comparable with the noise run being slightly higher on average. The specifications laid out by ATLAS allow a maximum noise occupancy of 5×10^{-4}. The mean values of noise occupancy for these runs were $(1.67 \pm 1.0) \times 10^{-4}$ and $(2.11 \pm 1.4) \times 10^{-4}$ respectively. The slight difference between the cosmic and noise runs could be due to false space points being formed and removed from the cosmic noise occupancy calculation. This can happen when both sides of a module fire within the allowed distance for a space point to be formed. Also, true spacepoints in the noise run will have been included in the calculation, increasing the overall level of noise. The actual noise occupancies are lower than that calculated. The method used to calculate the noise occupancy during calibration tests is more reliable since a known number of triggers are sent to each modules and the number of false hits is counted. Occupancies of the order of 10^{-5} were measured.

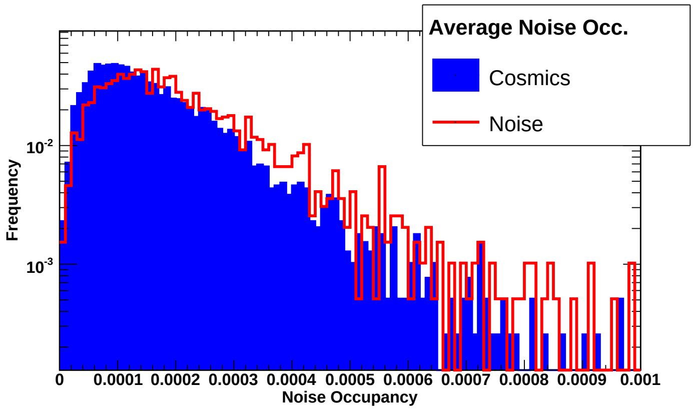


Figure 8.11: A comparison of the noise occupancy measurements taken during noise run 41912 and cosmic run 43719. The solid color denotes the cosmics run with a mean value $(1.67 \pm 1.0) \times 10^{-4}$. *The single line denotes the noise run with a mean value* $(2.11 \pm 1.4) \times 10^{-4}$.

Efficiency

The detector specifications require a module efficiency greater than 99%. In cosmic ray tests taken at the surface at CERN in 2006, module efficiencies were better than 99% [47]. The incident angle of cosmics (i.e. angle of incidence on a silicon sensor) is different from tracks that originate from the origin, and it has been shown that this can reduce the efficiency [46]. Figure 8.12 shows this dependence for the barrel surface cosmic run. A cut of 20° during track selection was introduced for the surface cosmics analysis. However for the M6 run, this cut was not enforced in the routine SCT monitoring software. This was to prevent losing valuable statistics for the early cosmic data.

To calculate the hit efficiency of the M6 run, the number of total hits was divided by the number of expected hits, summed over all events for the run. Since the hit rate was rather low for each module, the hit efficiency was calculated only for modules which had at least 8 reconstructed hits in total for the run (therefore dead or tripped modules were not counted). Figure 8.13 gives the results, showing a mean efficiency of 97% for all layers. The average of each layer is denoted with the errors representing the standard deviation for those modules in the layer. During the M6 run, there was no access to the module's condition database where known defects and information about the channels were available. Once the known module high voltage trips and defects are considered in the calculation, an increase in efficiency is expected.

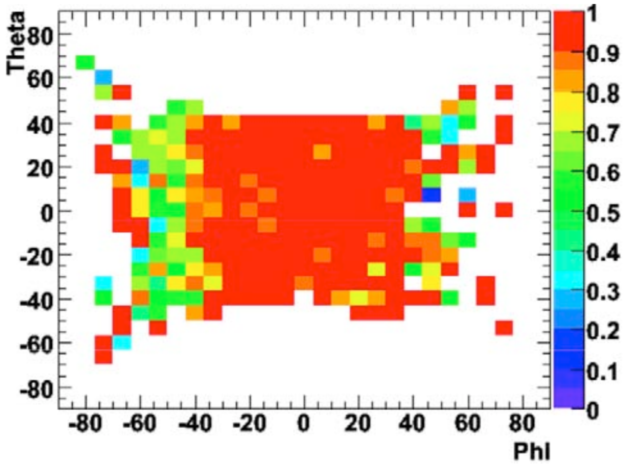


Figure 8.12: The efficiency as a function of theta and phi angles for the surface cosmic run (SR1).

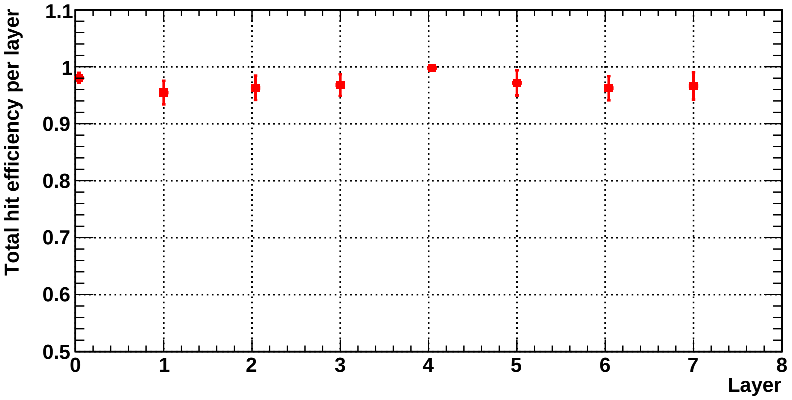


Figure 8.13: Module hit efficiencies per SCT barrel layer for M6 run. Only modules with more than 8 hits in total for the run were used in this analysis.

8.4 First beam

On 10^{th} September 2008 both proton beams were circulated individually around the 27 km circumference. The first events were recorded successfully within hours of the switch-on. Figure 8.14 shows the first event recorded by the ATLAS experiment. The beam was sent in stages around the ring, being stopped by different collimators. The event is the result of the beam interaction with the last collimator before the ATLAS experiment. ATLAS is the last experiment to be reached by the beam. The first beam performed three cycles and the second beam was circulated for several more. On Friday 19 September 2008, there was a failure of one of the magnets, resulting in a large helium leak into the LHC tunnel. Investigations indicated that the most likely cause of the problem was a faulty electrical connection between two magnets which probably melted at high current leading to mechanical failure. As a result of this, the LHC collisions are delayed until Summer 2009. To make use of the commissioning time up until the Winter shutdown, the ATLAS sub-detectors continued to commission with cosmics. This has allowed the inner detector endcaps as well as the pixel detector to participate. Figure 8.15 shows an event where a muon passes through the pixels, SCT and TRT detectors.

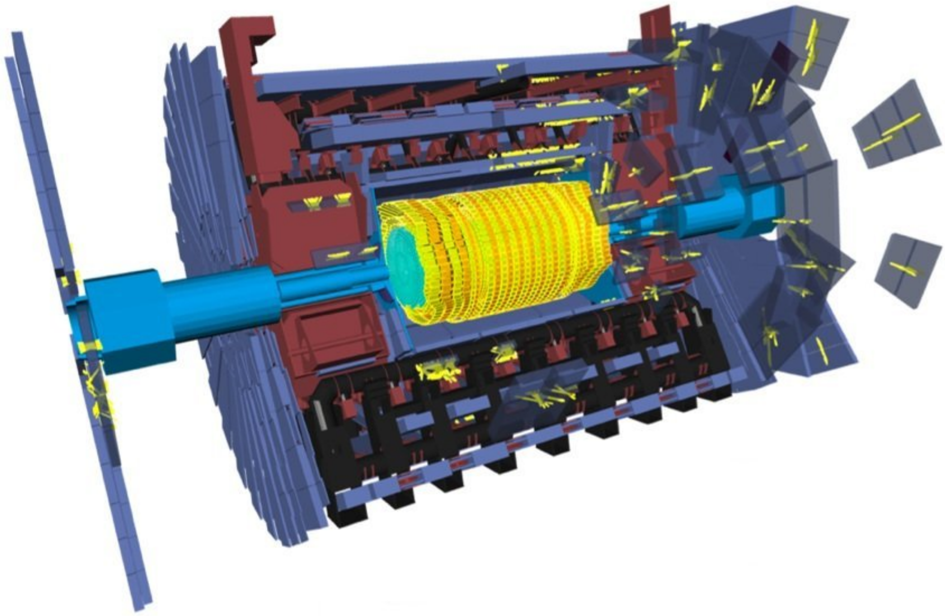


Figure 8.14: The first ATLAS event for the first beam circulated around the LHC ring. It deflects off the collimator sending a shower of muons through the Inner detector. Yellow represents a hit in the detector.

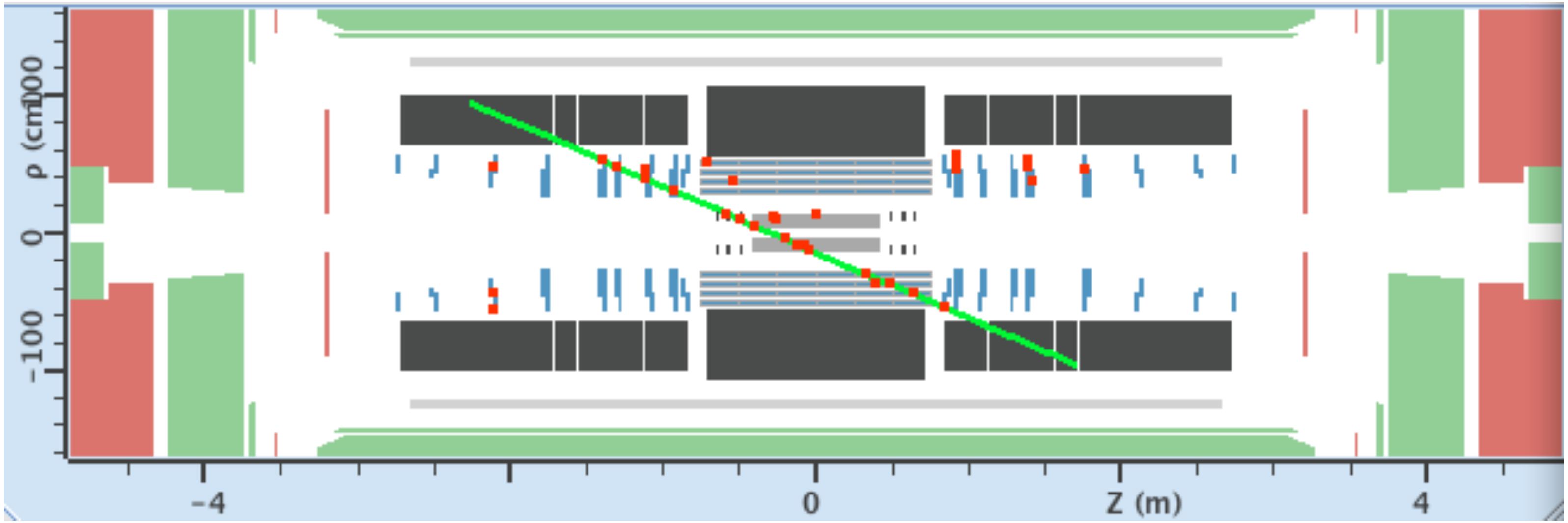


Figure 8.15: An event where a track goes through both SCT and TRT endcaps as well as the pixel detector. The Pixel detector is in light grey, the SCT in blue and the TRT in dark grey. The Pixel and SCT spacepoints are in red and the trackfit in green.

8.5 Conclusions and Outlook

The SCT Monitoring package is extremely important for monitoring all aspects of the module performance. The M6 run during March 2008 was the first opportunity to test the entire reconstruction software chain, as well as providing preliminary results on the detector performance and alignment. The time for commissioning the detector using cosmics was limited due to the number of problems which affected the cooling of the SCT (refer to section 5.4 for details). In August 2008 the SCT participated briefly in another global run just before the official switch-on of the LHC on September the 10^{th}. One single beam of protons was circulated fully around the 27 km tunnel through the individual LHC experiments. With first collisions not expected until Summer 2009, global commissioning with cosmic rays has resumed. Both the solenoid and toroid magnets were switched on, with deflected tracks being successfully reconstructed throughout the SCT detector and ATLAS sub-components.

Appendix A

Minimum Unit of Readout

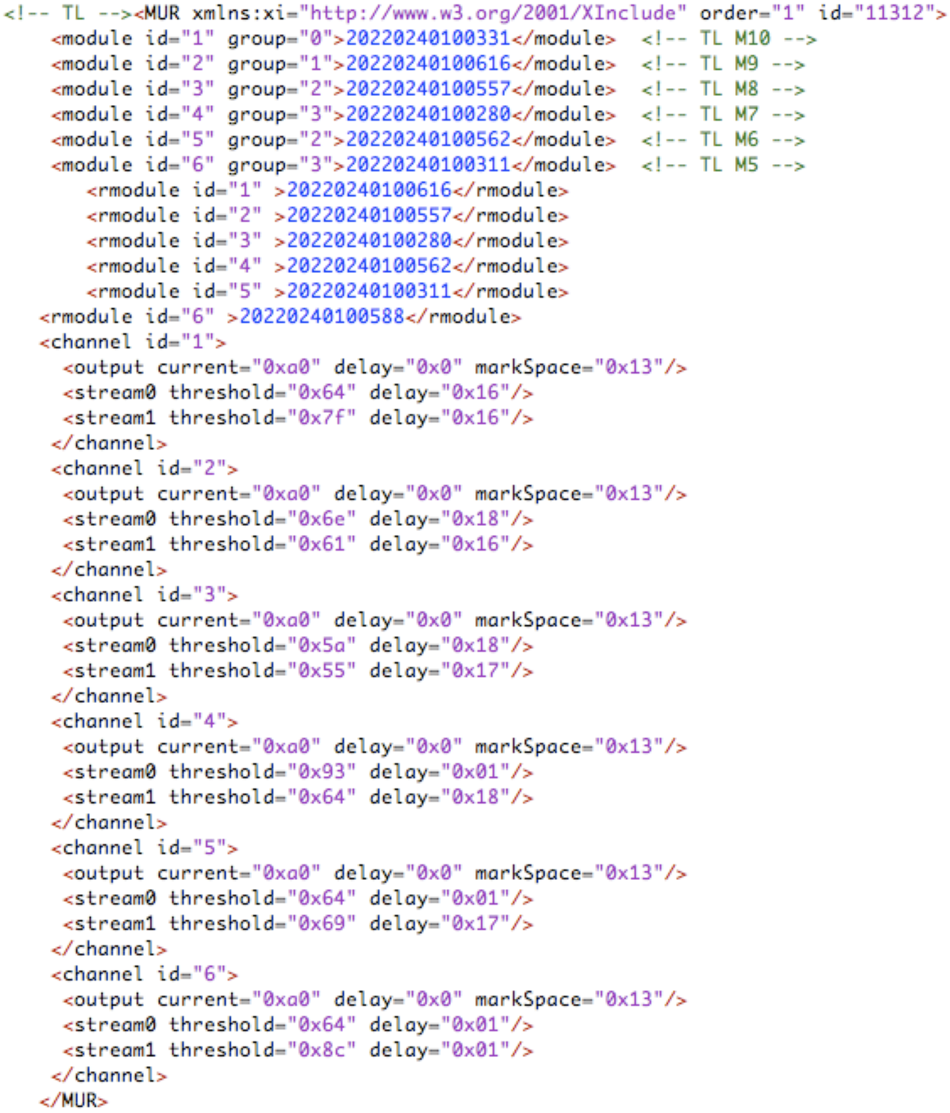
Each MUR contains a harness of a certain type. Table A.1 defines the harness types for the end-caps with their corresponding TX/RX ordering within each harness. In general, one harness can accommodate one eighth of the number of modules in a given ring. Harness HO3 is an exception since it picks up the remaining four O7 modules for disc 9. All the modules in a harness are assigned to a MUR.

TX	RX	HO1	HO2	HM1	HM2	HI1	HI2
0	0/1	O6		O7		I4	
1	2/3	O5		M4		I5	
2	4/5	O4		M3		I3	
3	6/7	O3		M2		I1	
4	8/9	O2		M1		I2	
5	10/11	O1		-		-	
6	0/1		O13		M10		I6
7	2/3		O12		M9		I8
8	4/5		O11		M8		I10
9	6/7		O10		M7		I7
10	8/9		O9		M6		I9
11	10/11		O8		M5		-

TX	RX	HO3
4	2/3	D9-BL-O7
5	4/5	D9-BR-O7
6	6/7	D9-TR-O7
7	8/9	D9-TL-O7

Table A.1: Overview of the harness types and their corresponding module-fibre mappings. One TX fibre can send data to a maximum of 12 modules. One RX fibre can read-out data from up to 6 modules. HO is for a harness with outers, HM is for a harness containing middles and Outer 7s (excluding disc 9), HI is for a harness containing inners. HO3 is a special harness picking up disc 9's outer 7's. The middle channels of the RX and TX fibres are used for the transmission and receiving of data.

Figure A.1 shows an example MUR file for Endcap-C. The modules associated to this MUR are located on disc 1, in the TL quadrant , on a harness containing middles, in the second position within the BOC. There is an *order* defining the RX plug-in position within the BOC and an *id* defining the type of modules associated to the harness and their position within each disc. The *id* is defined by a 5 digit number. Each of the digits represents a piece of information about the harness.



```
<!-- TL --><MUR xmlns:xi="http://www.w3.org/2001/XInclude" order="1" id="11312">
    <module id="1" group="0">2022024010033l</module>  <!-- TL M10 -->
    <module id="2" group="1">20220240100616</module>  <!-- TL M9 -->
    <module id="3" group="2">20220240100557</module>  <!-- TL M8 -->
    <module id="4" group="3">20220240100280</module>  <!-- TL M7 -->
    <module id="5" group="2">20220240100562</module>  <!-- TL M6 -->
    <module id="6" group="3">20220240100311</module>  <!-- TL M5 -->
       <rmodule id="1" >20220240100616</rmodule>
       <rmodule id="2" >20220240100557</rmodule>
       <rmodule id="3" >20220240100280</rmodule>
       <rmodule id="4" >20220240100562</rmodule>
       <rmodule id="5" >20220240100311</rmodule>
   <rmodule id="6" >20220240100588</rmodule>
   <channel id="1">
     <output current="0xa0" delay="0x0" markSpace="0x13"/>
     <stream0 threshold="0x64" delay="0x16"/>
     <stream1 threshold="0x7f" delay="0x16"/>
    </channel>
    <channel id="2">
     <output current="0xa0" delay="0x0" markSpace="0x13"/>
     <stream0 threshold="0x6e" delay="0x18"/>
     <stream1 threshold="0x61" delay="0x16"/>
    </channel>
    <channel id="3">
     <output current="0xa0" delay="0x0" markSpace="0x13"/>
     <stream0 threshold="0x5a" delay="0x18"/>
     <stream1 threshold="0x55" delay="0x17"/>
    </channel>
    <channel id="4">
     <output current="0xa0" delay="0x0" markSpace="0x13"/>
     <stream0 threshold="0x93" delay="0x01"/>
     <stream1 threshold="0x64" delay="0x18"/>
    </channel>
    <channel id="5">
     <output current="0xa0" delay="0x0" markSpace="0x13"/>
     <stream0 threshold="0x64" delay="0x01"/>
     <stream1 threshold="0x69" delay="0x17"/>
    </channel>
    <channel id="6">
     <output current="0xa0" delay="0x0" markSpace="0x13"/>
     <stream0 threshold="0x64" delay="0x01"/>
     <stream1 threshold="0x8c" delay="0x01"/>
    </channel>
   </MUR>
```

Figure A.1: An example MUR file for module configuration. This is for disc 1 in End-cap C, in the TL quadrant, with the 2^{nd} harness containing middle modules.

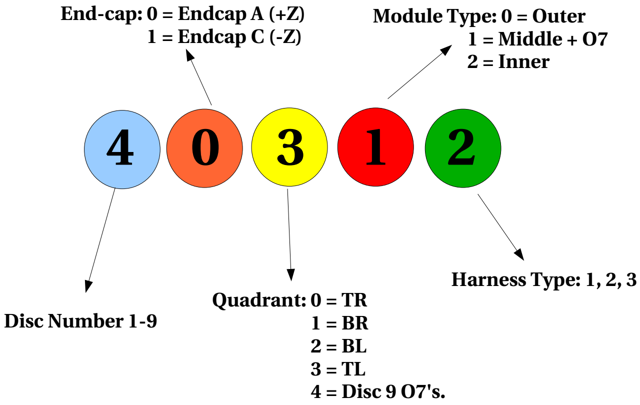


Figure A.2: Overview of the MUR identification notation. In this example a harness is positioned on disc 4, on Endcap-A, in the TL quadrant, with Middles, with harness type 2.

Figure A.2 provides a summary with the *id* nomenclature. As an example, a *MUR id* of 40312 represents a harness on *disc 4*, for *Endcap-A*, in the *BL quadrant*, with *middle modules*, on a *type 2* harness.

Included also in the MUR file is the *module id* and *group* with its associated TX and RX settings. The module *id* is the position of the module on the readout-harness. The group assigns a trigger group to the modules. Each ROD has four dedicated slave digital signal processors (DSPs) which send triggers to the modules in a group synchronously. In addition, modules in the same group have their data analysed and histogrammed on their assigned DSP.

There is an "*rmodule id*" that references the module that will receive the clock and command signal when operated in redundant mode. This is as a result of a module not being able to receive its own TTC signals. The *channel id* corresponds to the *module id*, representing the order of the module in the readout harness.

Next the settings for the output fibre sending the TTC signals to the module are defined. An output current is defined which sets the bias current of the *VCSEL* on the BOC. There is an associated delay which ensures that the local synchronisation (discussed earlier in 4.3.2) of modules is adjusted according to the TOF of particles from a collision at the IP. The mark-space ratio defines the duty cycle of the BPM-12 chip. Lastly the RX settings of the discriminator at the BOC for the two optical data streams 0 and 1 are defined.

Each module has its own configuration file which includes many elements. It contains the module serial number, which is a unique number identifying the object within the LHC project. For example a serial number 2022012800039, represents an ATLAS module (20), within the SCT detector (22) built at NIKHEF(12). Other file attributes include: whether a module is active, if the module is to be operated in TX redundant mode, chip id and hardware address, whether a chip is active, masking of specific channels, bypassing of chips, which readout mode, the trim range and which calibration line. Reference [30] gives a more detailed overview.

APPENDIX B

DETECTOR SETUP AND CALIBRATION TESTS

Various steps are taken to ensure that the modules are fully calibrated and optimised for readout during data taking. This includes optimisation of the optical links and internally calibrating the charge injection circuitry. A number of analogue and digital tests are performed on each module to ensure that the basic functionality of the readout chips are within specifications. The next sections will summarise the basic test phase of a full module characterisation. Here a brief overview of each test is given but for a more detailed review see reference [30].

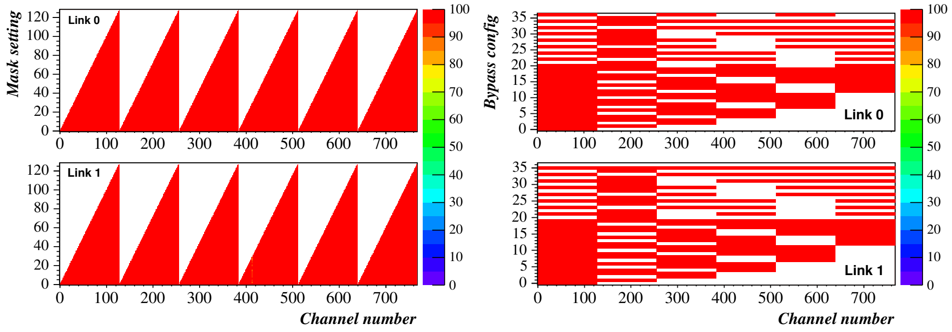
B.1 Optical Optimisation

RX Delay scan The timing of the BOC opto-receiver relative to the RX data signal is delayed in order to determine the optimum phase.

RX Threshold scan Triggers are sent to each module and the contents of the configuration registers are returned. This is repeated several times for the stability of results. If there are no bit errors then the correct data packet is returned. The discriminating threshold set by the DRX-12 ASIC at the BOC is varied using a Digital to Analogue Converter (DAC). It is scanned from 0 - 255 during each trigger burst. This allows a maximum and minimum receiving threshold to be set, for which there are no bit errors returned. The best value is taken to be 75% of the difference between the two values. (See Figure 4.10.)

2D BOC scan This is an extremely fast scan that combines both the RX delay and threshold scans into one. A further threshold scan is recommended in order to optimise the links further, especially when the 2D BOC analysis fails to provide optimum settings as a result of problematic slow-turn on links.

TX Current Scan This test finds the optimal TX settings for the *VCSELs* at the BOC sending the optical clock and command signals to the modules. If too high a setting is given, the DORIC on the module front-end can become saturated, causing errors in the data. By checking the current of the *p-i-n* diodes on the module, this can help assess if the TX settings are correctly set. If the currents on the diodes are too low,



(a) (b)

Figure B.1: Two tests to check the digital functionality of the ASICs. On the left (a) typical raw data plots for an Nmask test. On the right (b) a full bypass test.

then most probably the TX current can be set higher. Likewise if the *pin* currents are too high then the TX current can be reduced.

Mark Space Ratio Scan The duty cycle of the *VCSEL* optical signal needs to set to 50% in order to maintain a low clock jitter. The DORIC decodes the bi-phase mark encoded electrical signals output from the *pin* and creates the original clock pulses from both the leading and trailing edge of the 20 MHz clock. If the duty cycle is not equal to 50% there will be one group with a period longer than 25 ns and the other with a shorter period, creating a jitter in the clock [24].

Module Probe This test checks that the modules are returning events properly. If the optical communications are not optimal then this test should give an indication of the optical settings that still need to be tweaked to enable a stable performance from the modules.

B.2 Digital Tests

Hard Reset Test This test checks that the clock and command and hard reset signals are all functioning properly. A 40 MHz clock signal is sent to the modules and the master chip on each side of the module sends back this signal with a frequency divided by 2. Next the module is sent a configuration command, which results in the 20 MHz return signal being lost. Then a hard reset is issued, resetting the chips, so that the clock divided by 2 signal is once again returned.

Redundancy Test In the case that a module fails to receive its clock and command signals, a redundancy scheme exists whereby the clock and command signals can be sent from the neighbouring module instead. For both the primary and redundant modes, the chips must return their mask registers.

NMask Test Different mask register patterns are sent to each channel of a module. A defect will be recorded if a particular channel fails to be masked. Data is only returned for those channels that are not masked. Various mask register patterns of varying lengths are sent and the corresponding return data checked by the DAQ. This test relies greatly on the optical configuration being set at the most optimal values. If the test fails, it is usually as a result of the optical settings needing adjustment. Figure B.1 shows a typical raw plot for an Nmask and Full bypass test. On the left, the triangular shape represents the different lengths of sent data packets. Colour represents returned data. On the right, the module is programmed to each possible configuration of routing token and data between the chips.

Pipeline Test This tests if any of the cells in the pipeline for each channel are unresponsive (dead) or permanently outputting a 1 ("*stuck*".) Each pipeline is 132 cells deep, but they are ordered in 11 blocks, each with 12 cells. Each pipeline is cleared by a soft reset, followed by the injection of a known hit pattern into a given location. By varying the timing between the reset and the injection, different pipeline cells can be tested. The test is performed twice, once with all the channels on to identify dead cells, and a second time with the channels all off to identify the stuck cells. If all 12 cells are dead/stuck, then a defect of either dead or stuck is recorded. In any other case where the number of defective cells in a block is greater than 0 but less than 12, the defect name "*deadcell*" or "*stuckcell*" is issued.

Full Bypass Test As explained earlier in section 4.1.3, the chips on each module side are daisy chained together. The master chips receives the data from the other chips before sending the data to the RODs. In the event that one or more chips has a failure and cannot be readout, bypass links allow the routing of data around the chip. Each of the 62 possible chip combinations is tested. 100 trigger burst are sent to the module and the mask registers returned. After irradiation, a lower value of Vdd is required for the token passing between links. Therefore, several different values of Vdd ranging from 3.5-3.9 V is tested.

B.3 Analogue Tests

Strobe Delay Test The digital part of the ASIC looks at the output of the comparator at the rising edge of every clock cycle. A strobe delay scan varies the timing between the calibration pulse injection and the clock cycle. This optimises the timing of the injected charge, to avoid the non-readout of any hits that are present. A 4.0 fC charge is injected and the discriminator setting is at 2.0 fC. A strobe delay range of approximately two clock cycles, ranging from 0 - 63 is scanned. At each point, a charge is injected, a trigger sent and the channels readout. This is performed 1000 times producing a hit probability distribution over the entire tested range. Typically the window where a charge pulse is found, is approximately one clock cycle long (see Figure 4.3.) The strobe delay value is set to 40% along this active window and only one can be set for each chip.

3Pt Gain Test Injected charges of 1.5, 2.0, 2.5 fC are used during 3-Pt Gain threshold scans. The S-curves created allow the extraction of the VT_{50} points. A plot of the VT_{50} points versus injected charge allows the application of a linear fit. This allows the extraction of the slope (gain), intercept (offset) and computed input noise for all channels of a module.

Trim Range Scan Since only one discriminator threshold can be set for each chip, there are small variations in the channel to channel response and as a result, the discriminator offsets need to be corrected. This is achieved by adjusting the 4-bit trimDAC of each channel. There are four different trim ranges with 4 trimDAC settings. A series of 1fC threshold scans are performed for each trimDAC setting. The output VT_{50} points from the scans are plotted against their trimDAC values. The trimDAC value needed to reach the globally defined VT_{50} point is recorded. Next, the number of channels that are trimable for each trim range are calculated and the lowest range with the maximum number of trimmed channels is set for each chip. Any channel that cannot be trimmed is masked off and recorded as being defective.

Response Curve Test The 3-Pt Gain scan is a quick way of determining the input noise for each channel in a module. A response curve does essentially the same, except that it uses a larger number of injected charges for more accuracy. It is also performed once a module has been trimmed. Charges of 0.5, 0.75, 1.0, 1.25, 1.5, 2, 3, 4, 6, 8 fC are used. An exponential fit is used in determining the gain of each channel, compared to a linear fit which is used in the quicker 3-Pt gain test.

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SUMMARY

The Large Hadron Collider (LHC) has been built under the french-swiss border near Geneva, Switzerland. Two opposing beams of protons will collide with a centre of mass energy of 14 TeV, an energy seven million times that of the first accelerator. The LHC takes particle physics research to a new frontier. On September 10^{th} 2008, the first single pilot beam of 2×10^9 protons was circulated successfully through the entire LHC, with an injection energy of 0.45 TeV. The first collisions are expected in Summer 2009.

One of the experiments designed to search for new particle phenomena is the ATLAS experiment. This is a general purpose detector capable of detecting and measuring the broadest range of particle signals. At the heart of the ATLAS detector lies the SemiConductor Tracker (SCT). It is a central part of the inner detector providing precision measurements of particle trajectories over a large η range.

The work presented in this thesis focuses on the performance and commissioning of the SCT detector. For Endcap-A, which was constructed at Nikhef, the assembly and calibration test results are described extensively in this work. The commissioning run in 2008 used cosmic rays to analyse and verify that the performance of the barrels was within specifications.

The SCT uses silicon micro-strip technology, with the sensors produced by two different manufacturers: Hamamatsu and CiS. Hamamatsu produced all of the barrel sensors and 82.8 % of the installed end-cap sensors. The remainder were produced by CiS, forming the middle/inner module types. The current-voltage (IV) scans of the sensors during module production showed a clear moisture dependence in different environments. Due to the different field plate geometries of the sensor manufacturer the CiS sensors behaved differently in a dry environment. The modules produced by the latter suffered from an earlier onset of micro-discharge and higher leakage currents. This was as a result of using the non-field plate strip configuration (where the metal strip is narrower than the width of the p-implant.) Fortunately, this effect could be easily controlled, by training the sensor.

During 2004 and 2005 Nikhef constructed one of the SCT endcaps. Endcap-A has been extensively tested both at Nikhef during macro assembly and upon reception and integration at CERN. The endcap was successively installed, together with the TRT in its final position within the ATLAS cavern in May 2007. More than 98.7% of the optical links (used to communicate to and from the modules) were functional. The input noise to the amplifier of each module channel has been extensively tested from module production through to the final ATLAS installation. There were no significant changes in the noise even after all levels of transportation and integration. The grounding and shielding of the thermal enclosures as well as the connection to the TRT have proved highly efficient. After installation inside the ATLAS experiment 99.7% of the module channels are fully working, which is well within the specification of 1% allowed defective channels. The part of the detector made at Nikhef has only one dead and two problematic chips.

A noise model has been developed and tested with measured noise results for thirteen SCT modules. A simulation of this model also gives a breakdown of the overall contributions to the noise. The most dominating of sources is the noise in the amplifier due to the base spread resistance. The total-strip capacitance is the dominating factor in the sensor. It is known that the total-strip capacitance changes as a function of bias voltage, so this has been investigated and implemented in the noise model. A fit has been made to the measured data points with the best fit outputting the behavioural form of the total-strip capacitance. A method of constraining the behaviour of the total capacitance has been investigated. Performing a fit on all SCT modules gives a good approximation of the geometrical values of C_{tot}. On initial application of the bias voltage, the total-strip capacitance takes a certain time before it will stabilise. This feature will not be a problem during the running of ATLAS, since the detectors will have been biased for a longer period of time. Knowing the total-strip capacitance, the depletion voltage parameter can be released from the noise model. This provides an extremely useful method for tracking the radiation damage of the detector and giving an overall estimate of the lifetime of the detector.

The SCT Monitoring package is extremely important for monitoring all aspects of the module performance. The milestone 6 run during March 2008 was the first opportunity to test the entire reconstruction software chain, as well as providing preliminary results on the barrel detector performance and alignment. On September $10\mathrm{th}$, the LHC was officially switched on. During this time, events were recorded while a proton beam was circulating. For the remainder of 2008, the SCT continued to participate in global ATLAS cosmic runs.

SAMENVATTING

De ‘Large Hadron Collider’ (LHC) is gebouwd onder de Frans-Zwitserse grens bij Geneve, Zwitserland. Er zullen twee tegengestelde protonenbundels botsen met een totale zwaartepuntsenergie van 14 TeV, een energie die zeven miljoen keer zo groot is als die van de eerste versneller ooit. Met deze energie zoekt de LHC een nieuwe grens van de deeltjesfysica op. Op 10 september 2008 is de eerste bundel van 2×10^9 protonen met een injectie-energie van 0.45 TeV door de hele LHC gecirculeerd. De eerste botsingen worden verwacht in de zomer van 2009.

Een van de experimenten die ontworpen is om naar nieuwe fenomenen te zoeken, is het ATLAS experiment. Dit is een multifunctionele detector, die een breed scala aan fysicasignalen kan detecteren. Het hart van de ATLAS detector is de ‘SemiConductor Tracker’ (SCT). Dit is een centraal onderdeel van het binnenste gedeelte van de detector en voorziet in precisiemetingen van deeltjesbanen over een groot η-bereik.

Het werk dat in dit proefschrift gepresenteerd wordt, richt zich op het functioneren en de ‘commisioning’ van de SCT detector. Voor Endcap-A, die gebouwd is op Nikhef, worden de montage en de calibratietests uitgebreid beschreven. De commisioning run uit 2008, met kosmische stralen, is geanalyseerd om te verifiëren dat het functioneren van de ‘barrels’ binnen de specificaties viel.

De SCT gebruikt silicium micro-strip technologie. De sensoren zijn geproduceerd door twee verschillende fabrikanten: Hamamatsu en CiS. Hamamatsu heeft alle barrelsensoren geproduceerd en 82.8 % van de geïnstalleerde end-cap sensoren. De overige sensoren zijn geproduceerd door CiS. Dit zijn de middelste/binnenste typen modules. De stroom/spanning (IV) metingen van de sensoren gedurende de productie van de modules lieten een duidelijke vochtafhankelijkheid zien in verschillende omgevingen. Door de andere ‘field plate’ geometrieën van de sensorfabrikant gedroegen de CiS sensoren zich anders in een droge omgeving. Deze modules hadden eerder last van micro-ontlading en hogere lekstromen. Dit werd veroorzaakt doordat de ’non-field plate strip’ configuratie werd gebruikt (waar de metalen strip dunner is dan de breedte van de p-laag). Gelukkig kan dit effect gemakkelijk tegengegaan worden door de sensor te trainen.

Gedurende 2004 en 2005 heeft het Nikhef een van de SCT endcaps gebouwd. Endcap-A is uitgebreid getest, zowel bij de macro-montage op het Nikhef als bij de ontvangst en integratie op CERN. De endcap en de TRT zijn succesvol geïnstalleerd op de uiteindelijke positie in de ATLAS hal in mei 2007. Meer dan 98.7% van de optische links waren functioneel. De ingangsruis naar de versterker van ieder modulekanaal is uitgebreid getest, van de moduleproductie tot aan de uiteindelijke ATLAS installatie. Zelfs na alle vervoer en integratiestappen waren er geen significante veranderingen in de ruis. De aarding en afscherming van de isolatielaag en de connectie naar de TRT hebben bewezen zeer effectief te zijn. Na installatie in het ATLAS experiment werkt 99.7% van de modulekanalen goed, hetgeen ruim binnen de specificatie van 1% toegestane defecte kanalen valt. Het deel van de detector dat op Nikhef gemaakt is, heeft maar één dode en twee problematische chips.

Een ruismodel is ontwikkeld en getest met de gemeten resultaten van de ruis van dertien SCT modules. Een simulatie van dit model geeft ook een opsplitsing van de afzonderlijke ruisbijdragen. De belangrijkste bron is de ruis in de versterker die veroorzaakt wordt door de 'base spread resistance'. In de sensor is de inter-strip capaciteit de belangrijkste factor. Het is bekend dat de inter-strip capaciteit afhankelijk is van de bias-spanning, dus dit is onderzocht en geïmplementeerd in het ruismodel. Er is een fit gemaakt aan de gemeten datapunten waarbij de beste fit de vorm van de inter-strip capaciteit geeft. Er is een methode onderzocht om de invloed van de totale capaciteit te isoleren. Door een dergelijke fit uit te voeren op alle SCT modules, is een goede benadering van de geometrische waarden van C_{tot} te verkrijgen. Als de bias-spanning wordt aangezet, duurt het een bepaald tijd voor de inter-strip capaciteit gestabiliseerd is. Dit zal geen probleem zijn bij metingen in ATLAS, omdat de bias-spanning dan voor langere tijd op de detectoren staat. Als de inter-strip capaciteit bekend is, kan de parameter voor de uitputtingsspanning afgeleid worden uit het model. Dit geeft een zeer nuttige methode om de stralingsschade in de detector bij te houden en om een schatting van de levensduur van de detector te geven.

Het SCT monitoringpakket is erg belangrijk om alle aspecten van het functioneren van de modules te monitoren. De 'milestone 6' run in maart 2008 was de eerste mogelijkheid om de volledige reconstructiesoftwareketen te testen en om voorlopige resultaten voor het functioneren en de uitlijning van de barrel detector te krijgen. Op 10 september is de LHC officieel aangezet en zijn events vastgelegd terwijl de protonbundel circuleerde. In de rest van 2008 is de SCT blijven deelnemen aan algemene ATLAS runs met kosmische stralen.

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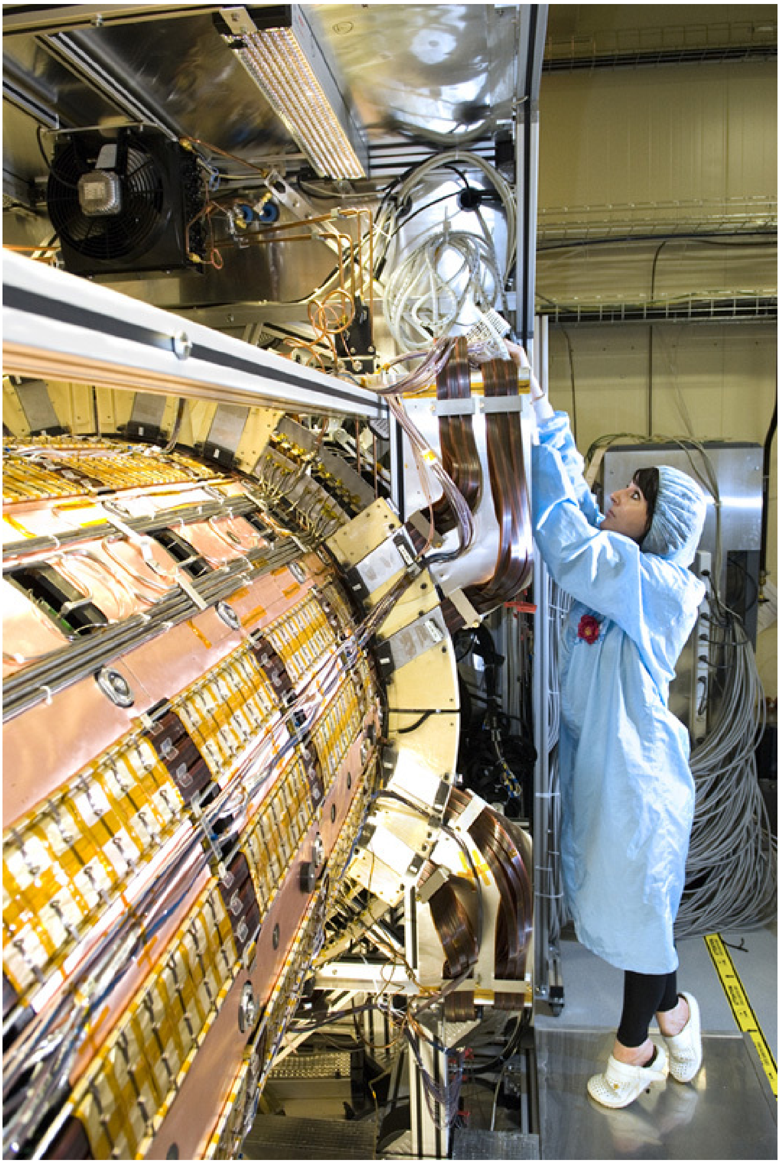
Caroline
Elst Gld, Feb 2009.

CURRICULUM VITAE

Caroline Magrath is an Experimental Research Physicist. She was born in Northern Ireland in 1982. She received five Grade A Highers in 1999 from the High school of Stirling in Scotland and was accepted to study Physics at the University of Glasgow. In 2002 she was selected to work as a Summer intern at the European Centre for Nuclear Research (CERN), in Geneva Switzerland. She worked on the ATLAS experiment on the Semi-Conductor Tracker (SCT) Barrel System-test. Her work involved testing prototype hybrids as well as performing investigative studies of electronic noise on irradiated and non-irradiated silicon modules. After completing her degree in 2003, with an Upper Second class Honours, she moved to Amsterdam to work at the National Institute for Subatomic Physics (Nikhef). She worked as a Research Technician for the Semi-Conductor Tracker group within Nikhef, assembling and commissioning Endcap-A of the SCT detector. She successfully quality assured and tested the hybrid and silicon wafers used to build 100 silicon detector modules. She also performed acceptance tests of the opto-electronic components for the Endcap detector. After working for nine months, Nikhef offered her the position of PhD Research Assistant and she continued her work with the SCT group, on the assembly and testing the Silicon Endcap. In March 2006 she moved to CERN as a Scientific Associate to help with the commissioning and integration of the Endcap within the ATLAS experiment. She was heavily involved in the reception tests both before and after installation in the ATLAS cavern. She also participated in data taking shifts during cosmic data taking periods. In November 2007 she returned to the Netherlands where she continued her thesis work at the Radboud University in Nijmegen. She was an author on several SCT and ATLAS publications and also participated in international conferences. This is her thesis on the Heart of the ATLAS detector, with the main focus on the Commissioning and Performance of the ATLAS Silicon Tracker.



The author of this thesis working on the reception testing of Endcap-A.